

FIG. 1

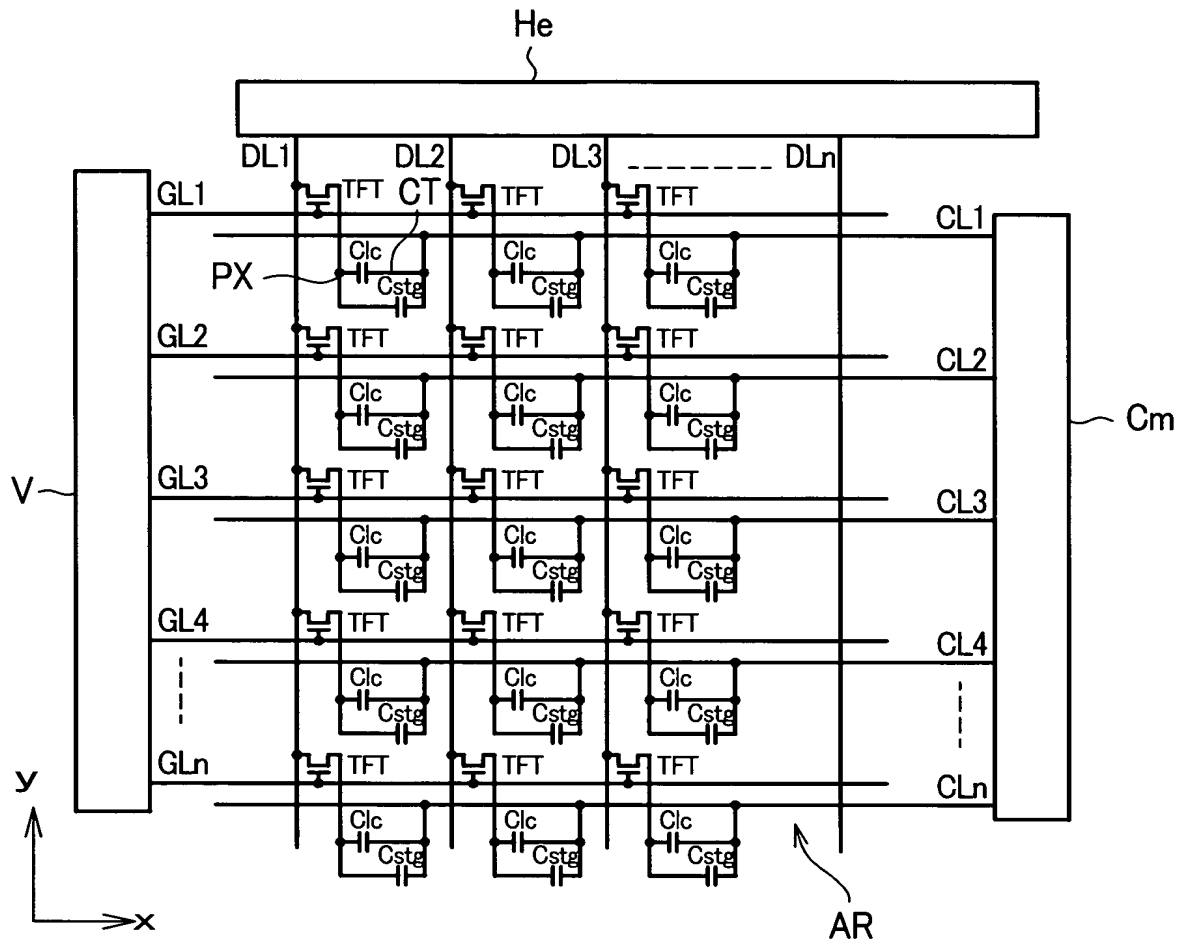


FIG. 2

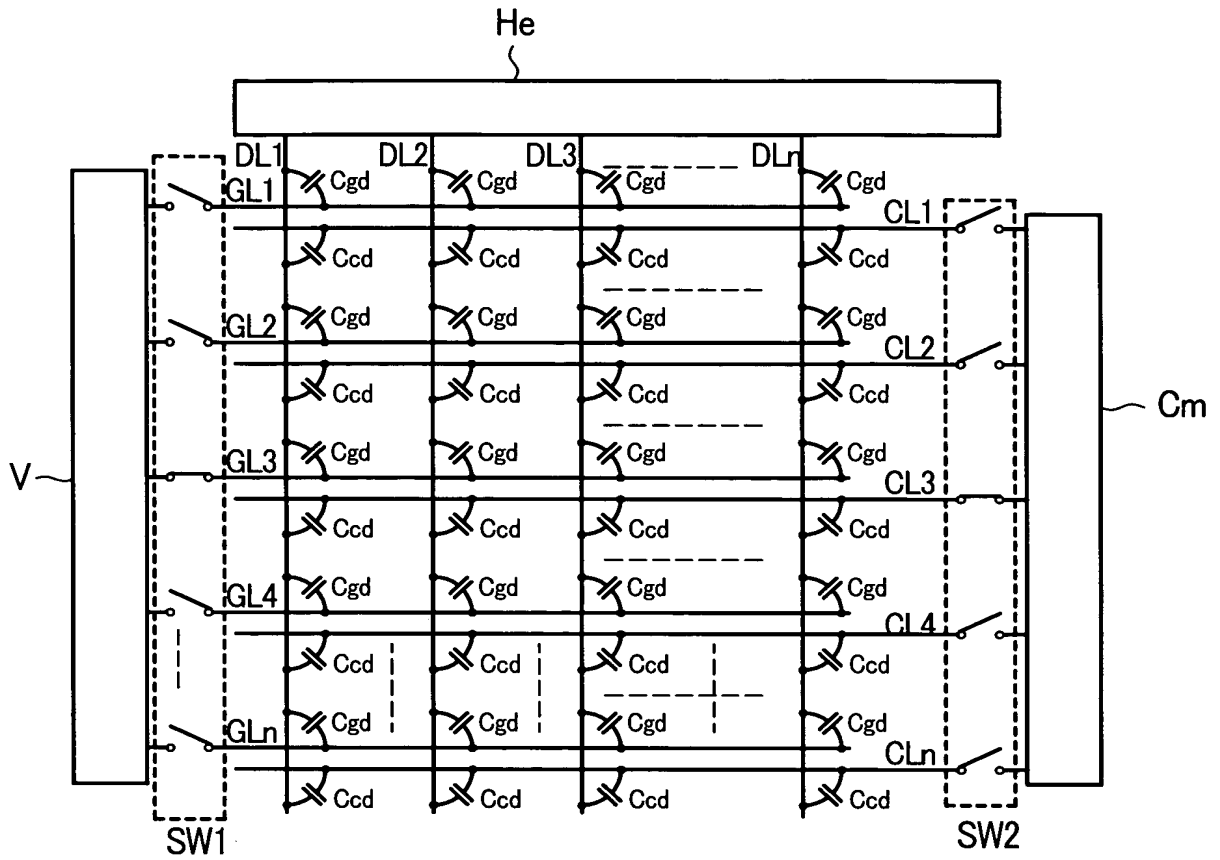
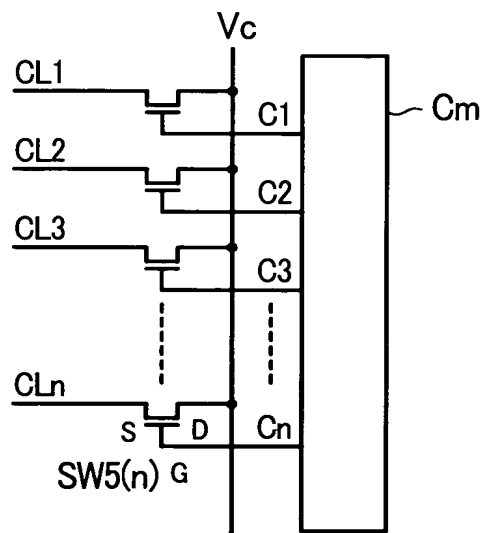


FIG. 4



Gn	ON	OFF	OFF	OFF
Gn+1	OFF	ON	OFF	OFF
Gn+2	OFF	OFF	ON	OFF
GLn	ON	OFF	FT	FT
GLn+1	FT	ON	OFF	FT
GLn+2	FT	FT	ON	OFF
SW1(n)	ON	OFF	OFF	OFF
SW1(n+1)	OFF	ON	OFF	OFF
SW1(n+2)	OFF	OFF	ON	OFF
SW2(n)	OFF	ON	OFF	OFF
SW2(n+1)	OFF	OFF	ON	OFF
SW2(n+2)	OFF	OFF	OFF	ON

A step function diagram. The signal is 'ON' for a duration labeled 'FT' and 'OFF' for a duration labeled 'OFF'.

FIG. 5A

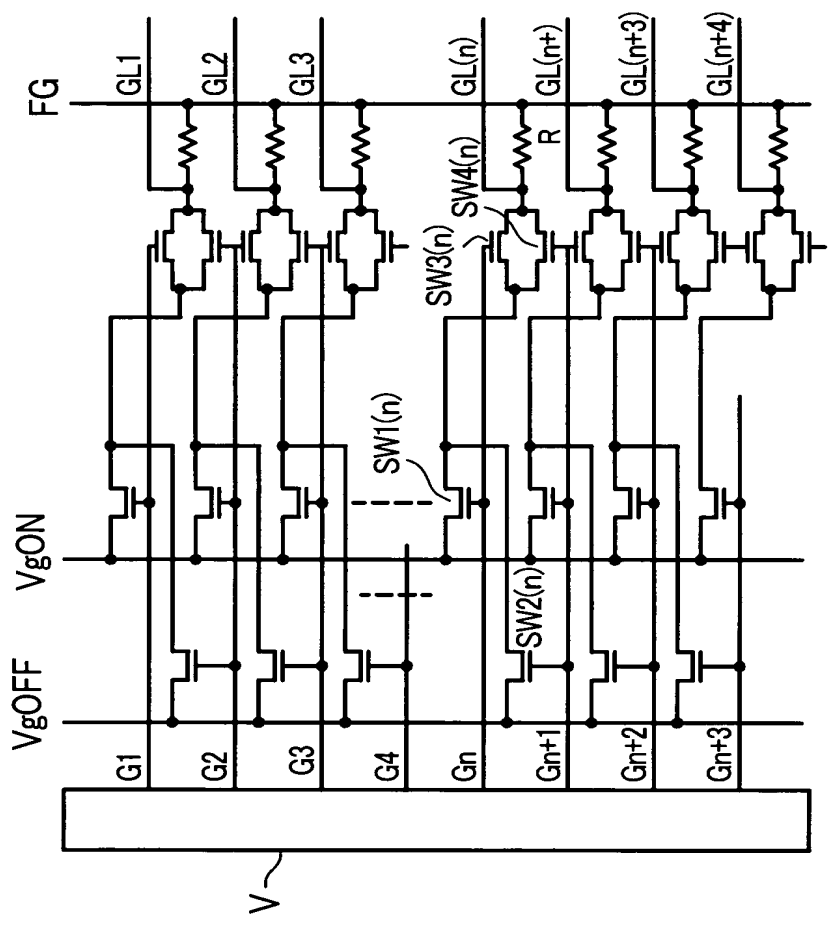


FIG. 5B

Gn	ON	OFF	OFF	OFF
Gn+1	OFF	ON	OFF	OFF
Gn+2	OFF	OFF	ON	OFF
Gn+3	OFF	OFF	OFF	ON
GLn	ON	OFF	FT	FT
GLn+1	FT	ON	OFF	FT
GLn+2	FT	FT	ON	OFF
GLn+3	FT	FT	FT	ON
SW1(n)	ON	OFF	OFF	OFF
SW2(n)	OFF	ON	OFF	OFF
SW3(n)	ON	OFF	OFF	OFF
SW4(n)	OFF	ON	OFF	OFF
SW1(n+1)	OFF	ON	OFF	OFF
SW2(n+1)	OFF	OFF	ON	OFF
SW3(n+1)	OFF	ON	OFF	OFF
SW4(n+1)	OFF	OFF	ON	OFF
SW1(n+2)	OFF	OFF	OFF	ON
SW2(n+2)	OFF	OFF	ON	OFF
SW3(n+2)	OFF	OFF	ON	OFF
SW4(n+2)	OFF	OFF	OFF	ON

FIG. 6

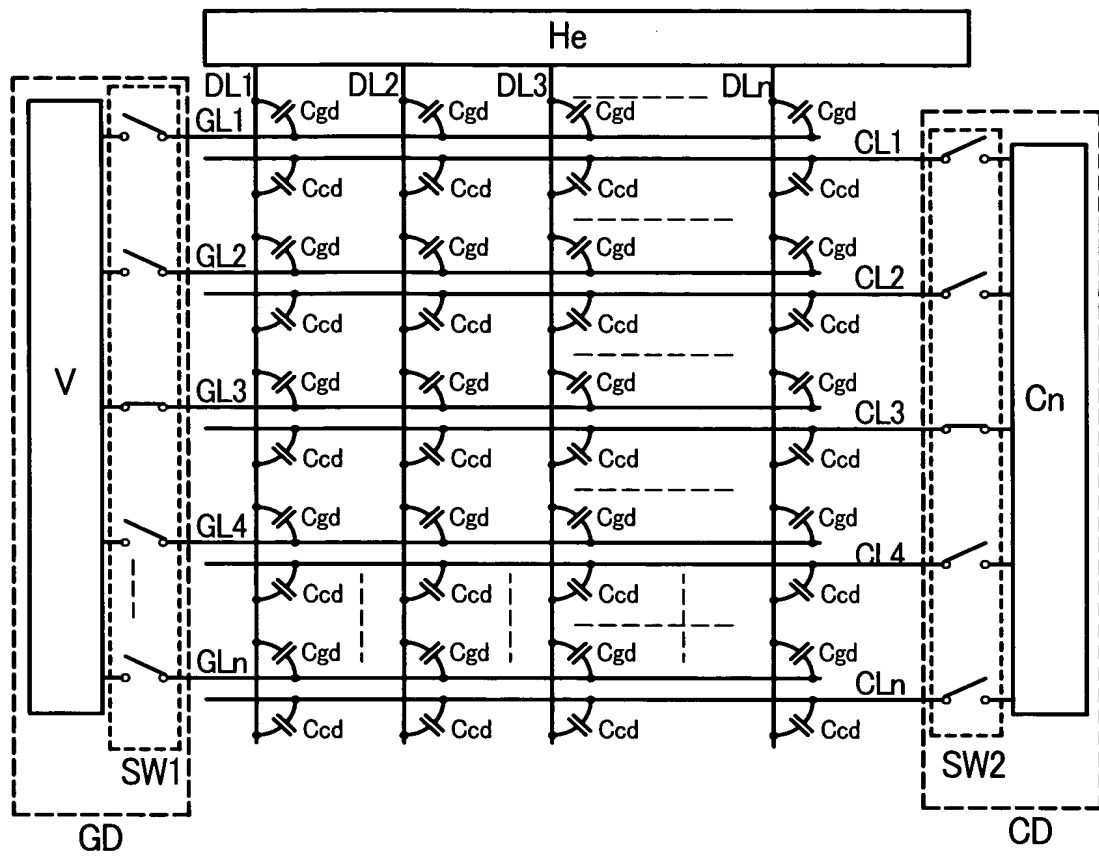


FIG. 7A

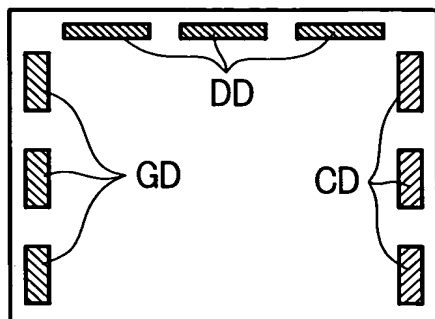


FIG. 7B

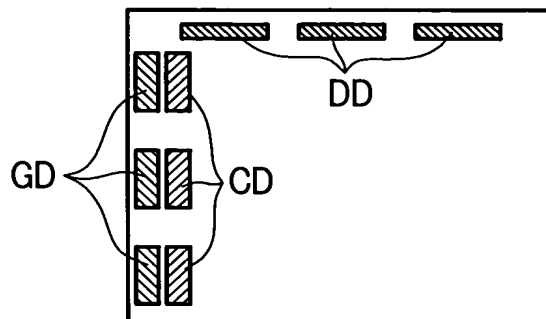


FIG. 7C

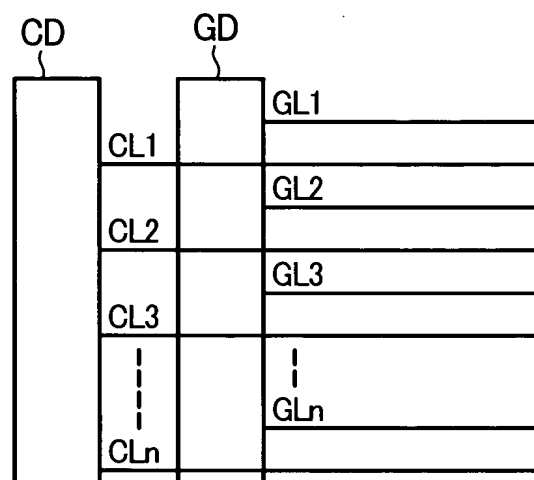


FIG. 8A

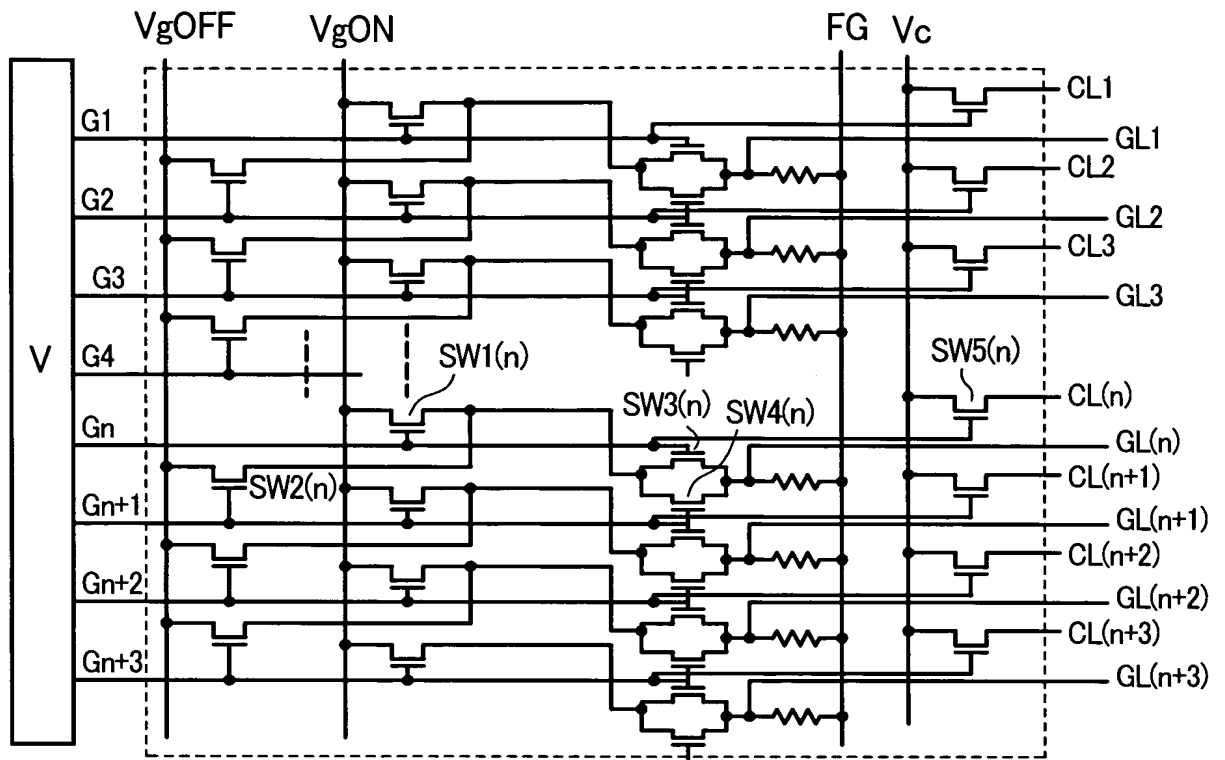


FIG. 8B

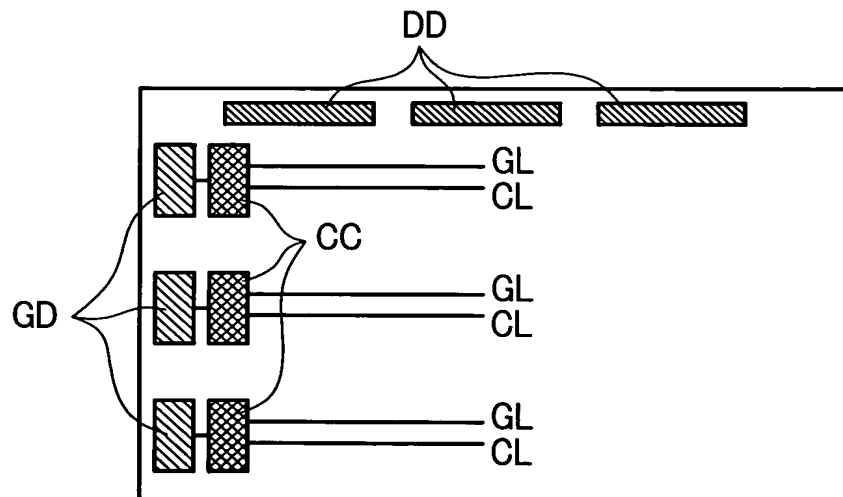


FIG. 9

G _n	ON	OFF	OFF	OFF
G _{n+1}	OFF	ON	OFF	OFF
G _{n+2}	OFF	OFF	ON	OFF
G _{n+3}	OFF	OFF	OFF	ON
G _{L_n}	ON	OFF	FT	FT
G _{L_n+1}	FT	ON	OFF	FT
G _{L_n+2}	FT	FT	ON	OFF
C _{L_n+3}	FT	FT	FT	ON
C _{L_n}				
C _{L_n+1}				
C _{L_n+2}				
C _{L_n+3}				
SW1(_n)	ON	OFF	OFF	OFF
SW2(_n)	OFF	ON	OFF	OFF
SW3(_n)	ON	OFF	OFF	OFF
SW4(_n)	OFF	ON	OFF	OFF
SW5(_n)	ON	OFF	OFF	OFF
SW1(_n +1)	OFF	ON	OFF	OFF
SW2(_n +1)	OFF	OFF	ON	OFF
SW3(_n +1)	OFF	ON	OFF	OFF
SW4(_n +1)	OFF	OFF	ON	OFF
SW5(_n +1)	OFF	ON	OFF	OFF
SW1(_n +2)	OFF	OFF	ON	OFF
SW2(_n +2)	OFF	OFF	OFF	ON
SW3(_n +2)	OFF	OFF	ON	OFF
SW4(_n +2)	OFF	OFF	OFF	ON
SW5(_n +2)	OFF	OFF	ON	OFF

FIG. 10A

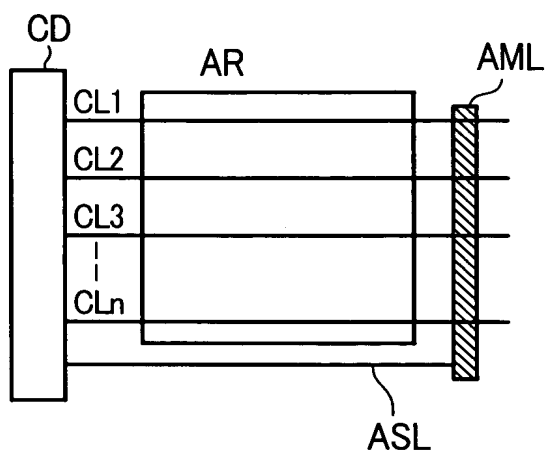


FIG. 10B

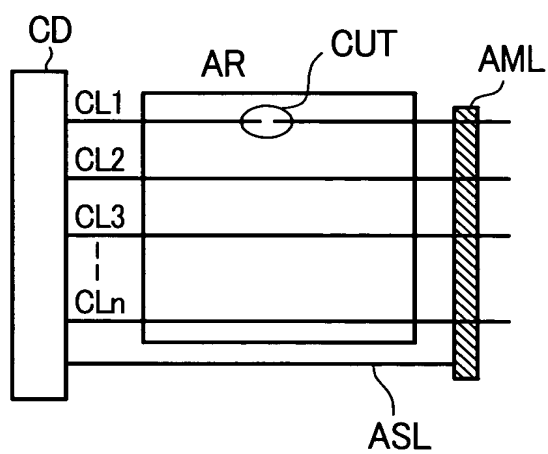


FIG. 10C

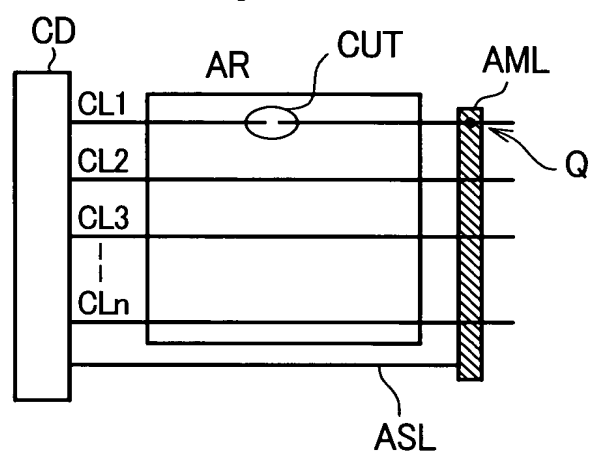


FIG. 11

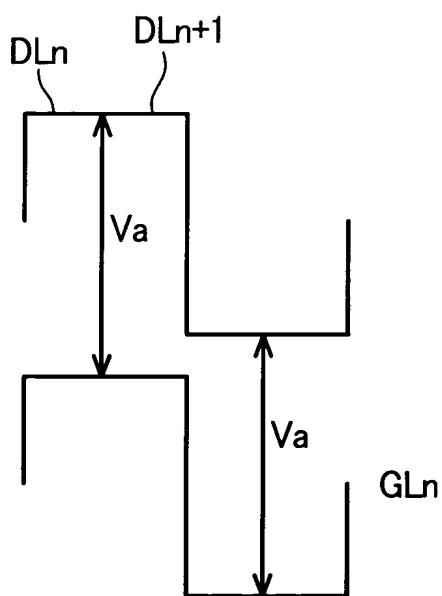


FIG. 12

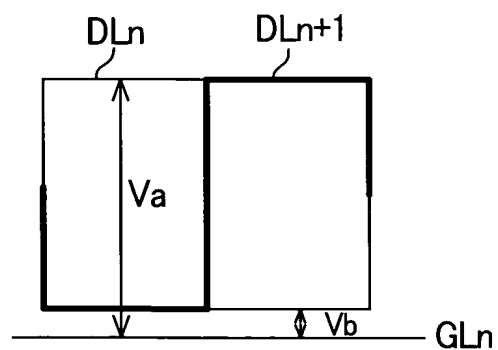


FIG. 13A

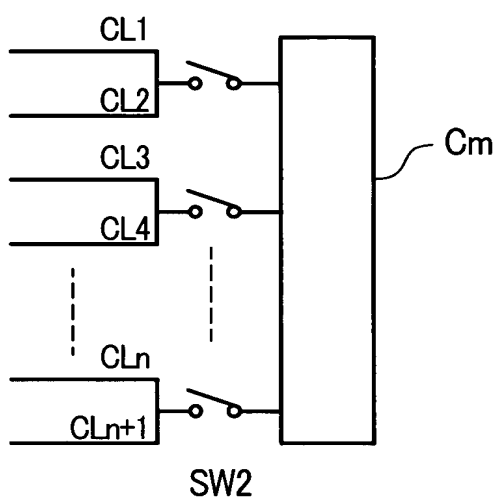


FIG. 13B

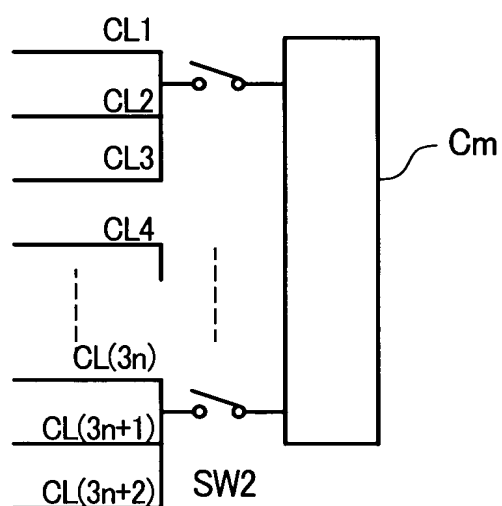


FIG. 13C

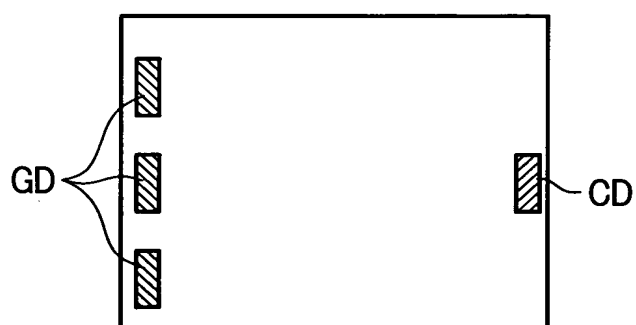


FIG. 14A

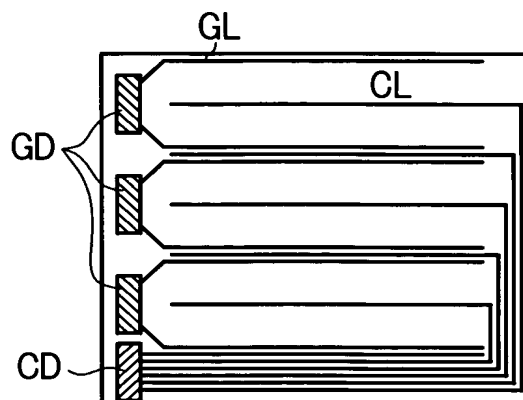


FIG. 14B

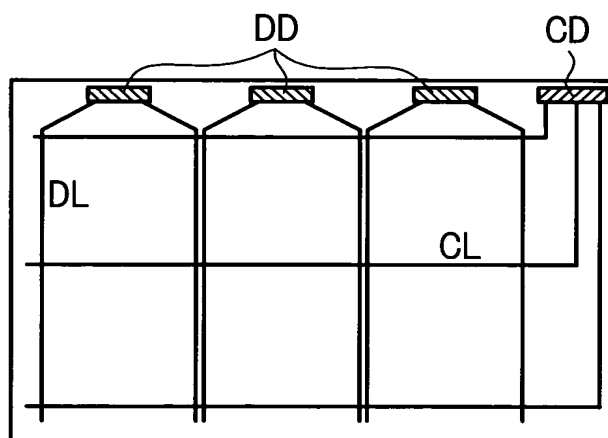


FIG. 15A

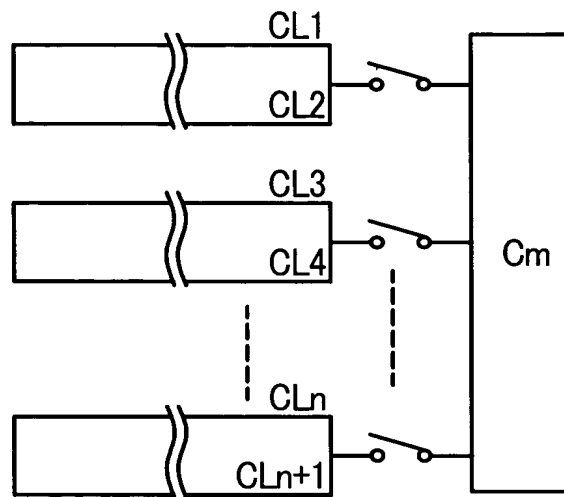


FIG. 15B

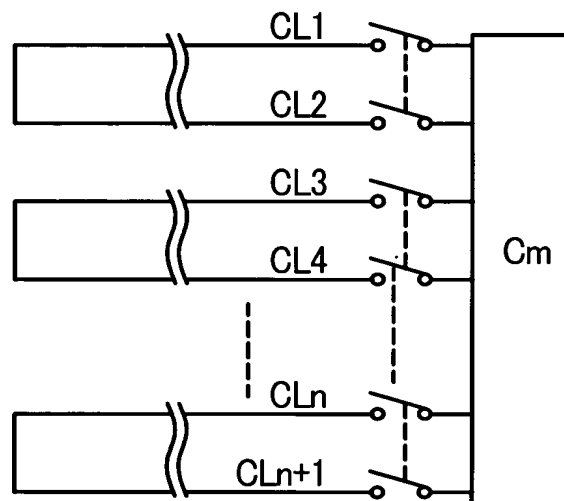


FIG. 16A

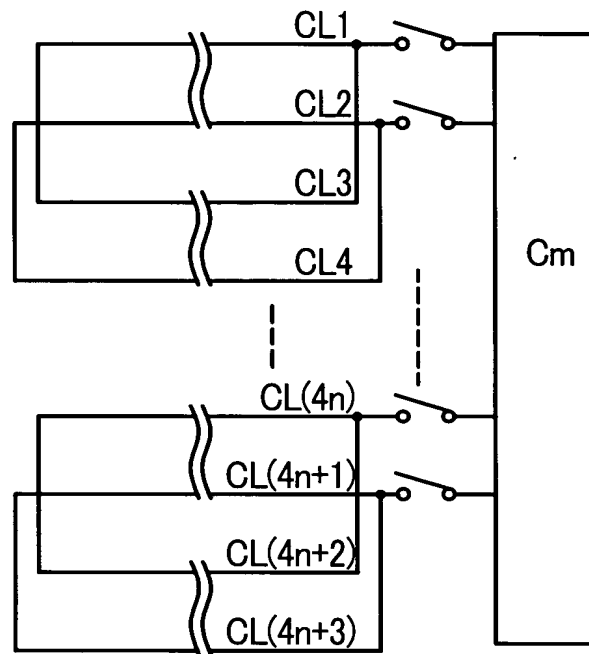


FIG. 16B

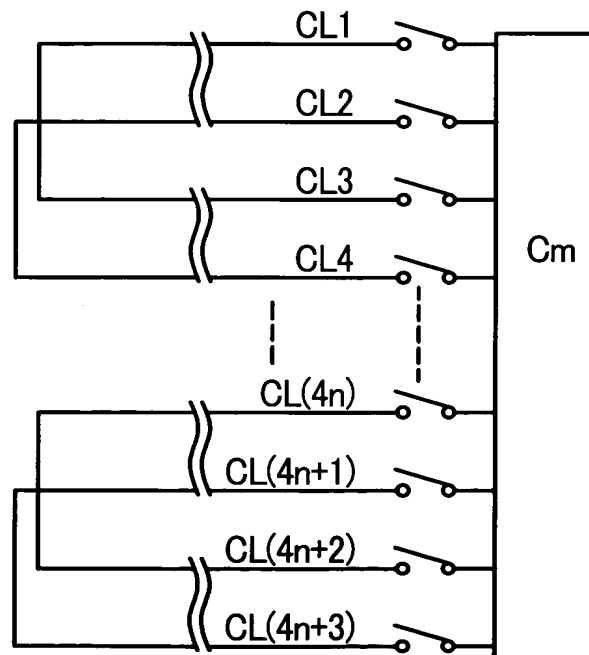


FIG. 17A

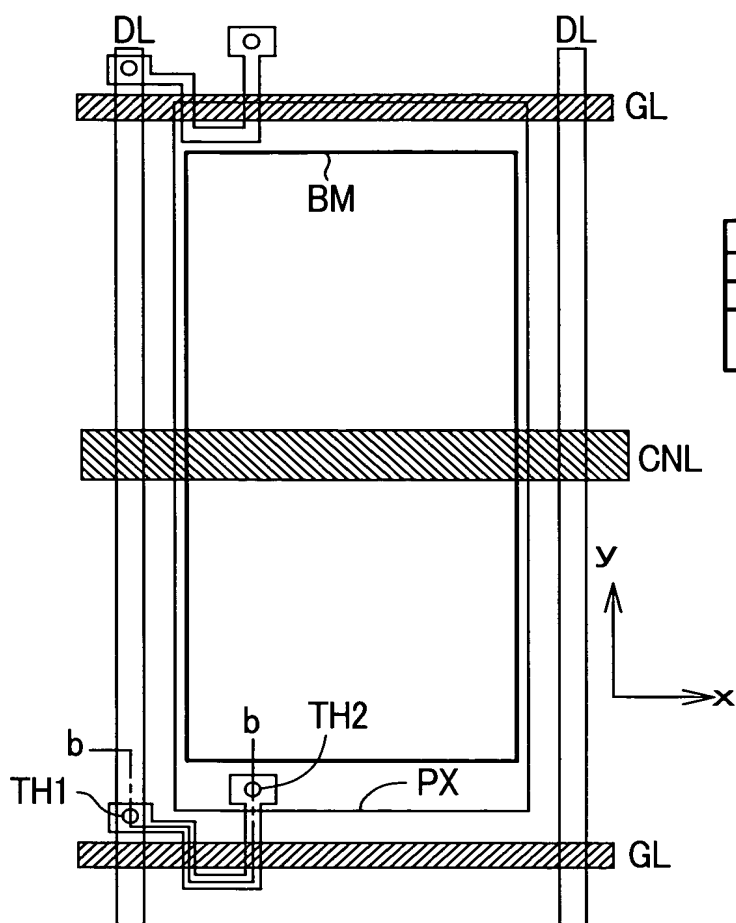


FIG. 17B

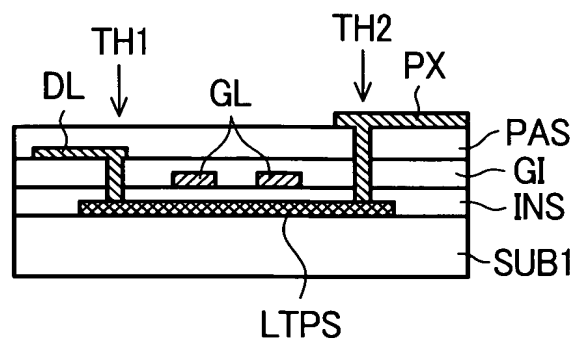


FIG. 18A

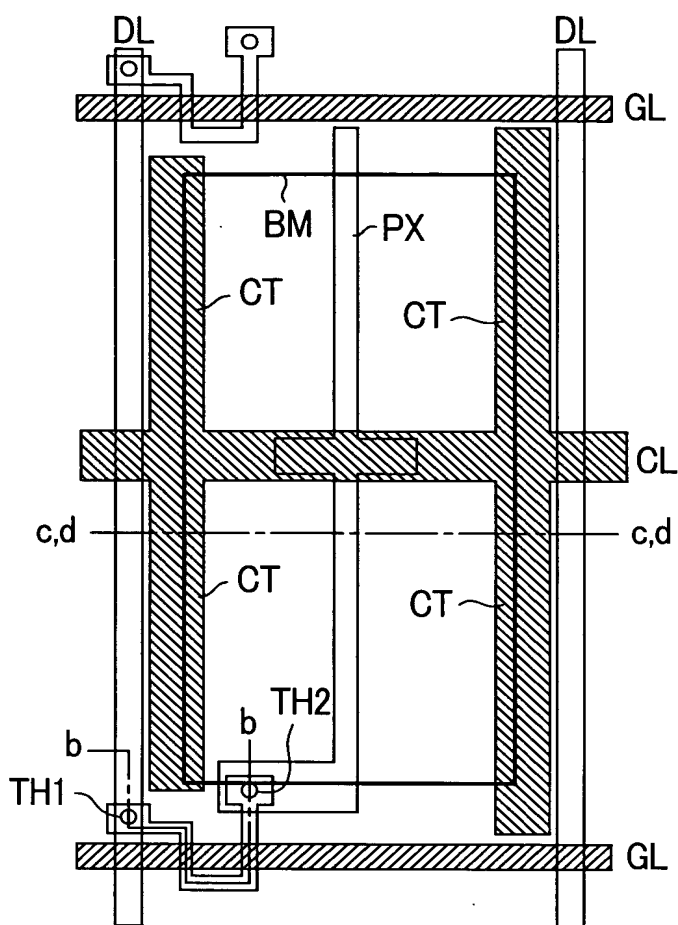


FIG. 18B

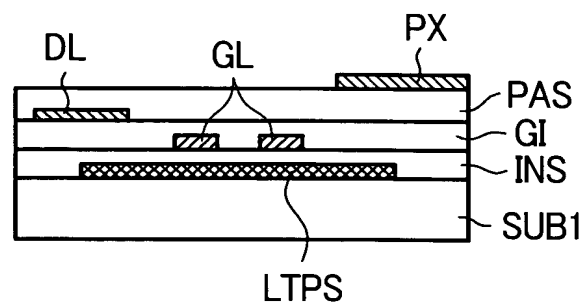


FIG. 18C

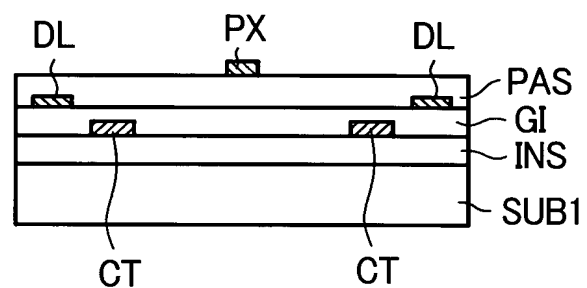


FIG. 18D

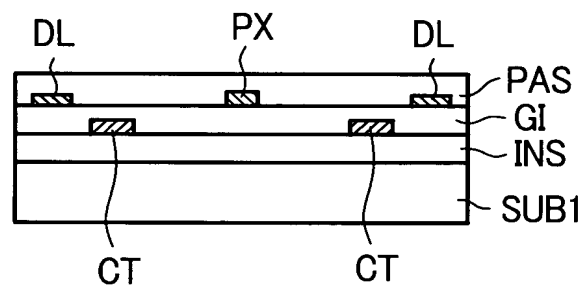


FIG. 19A

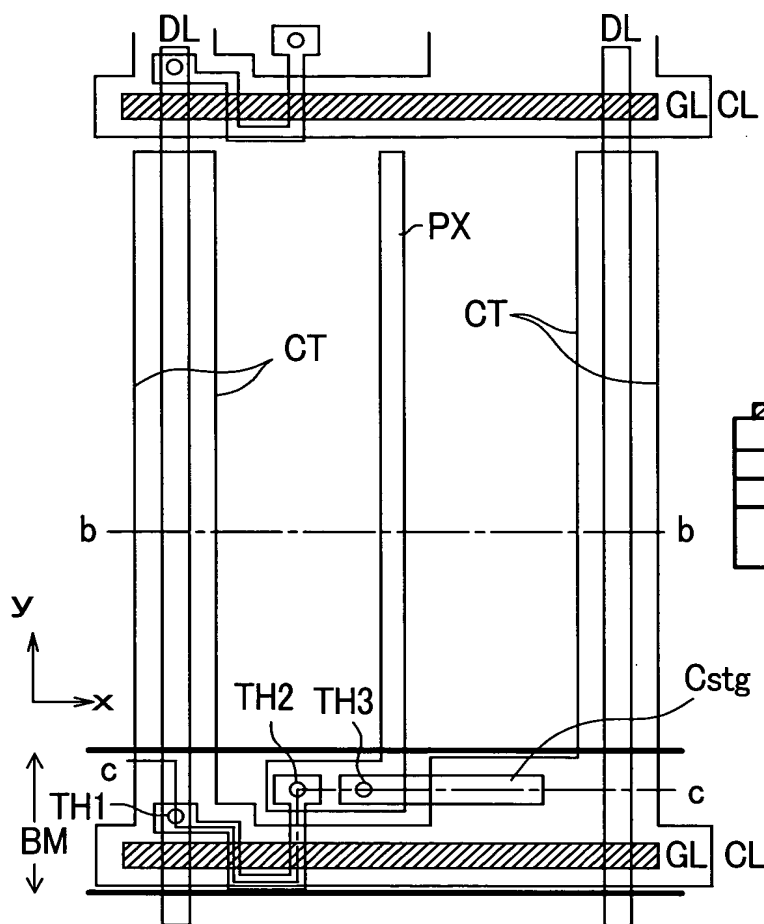


FIG. 19B

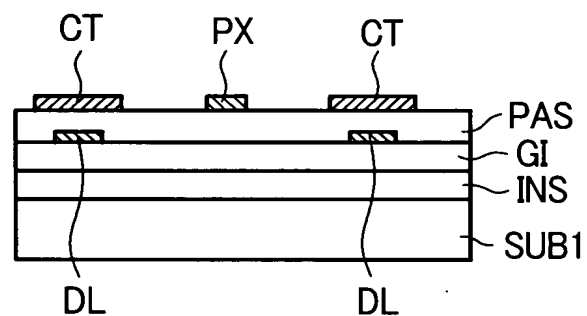


FIG. 19C

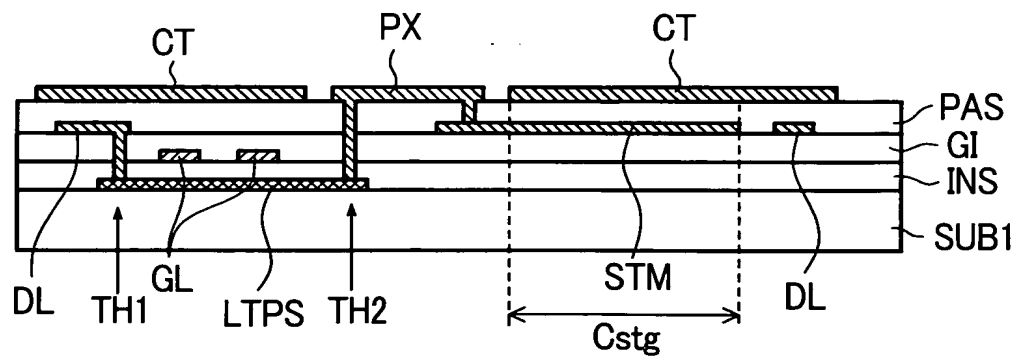


FIG. 20A

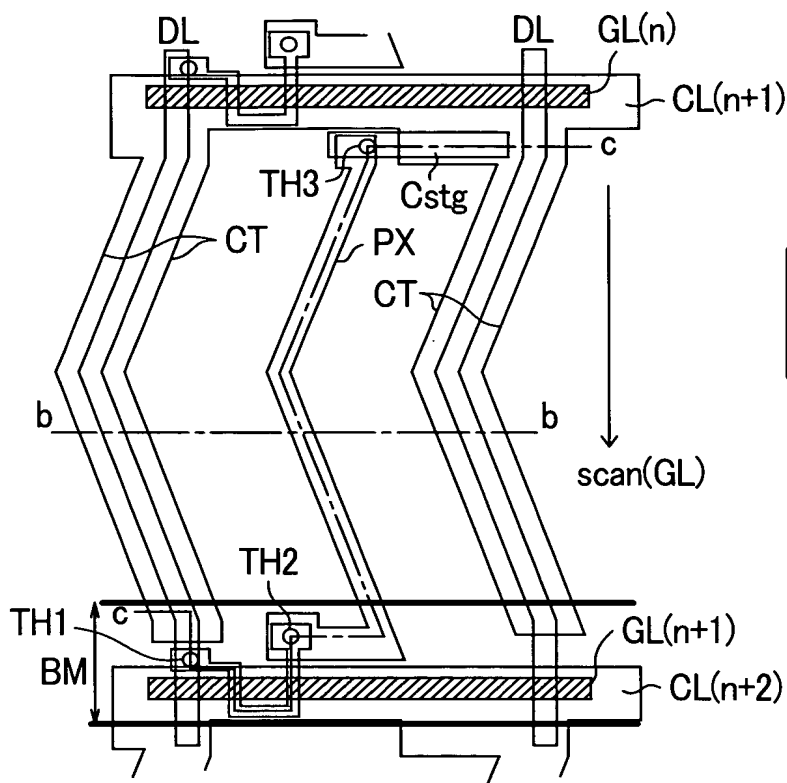


FIG. 20B

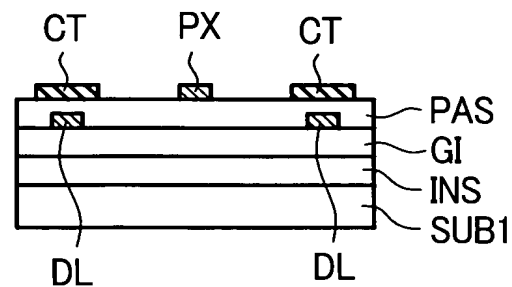


FIG. 20D

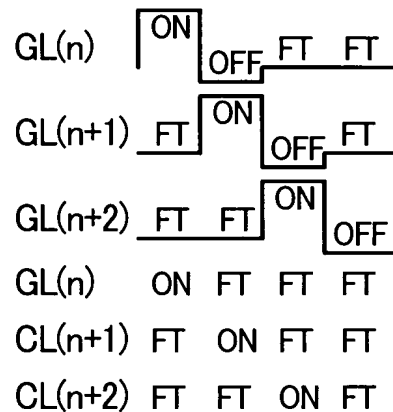


FIG. 20C

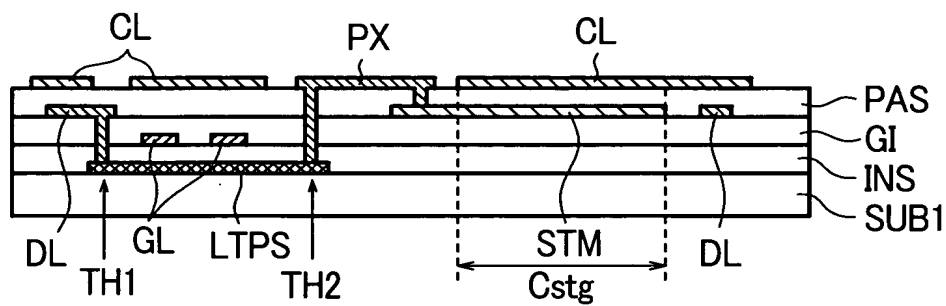


FIG. 21A

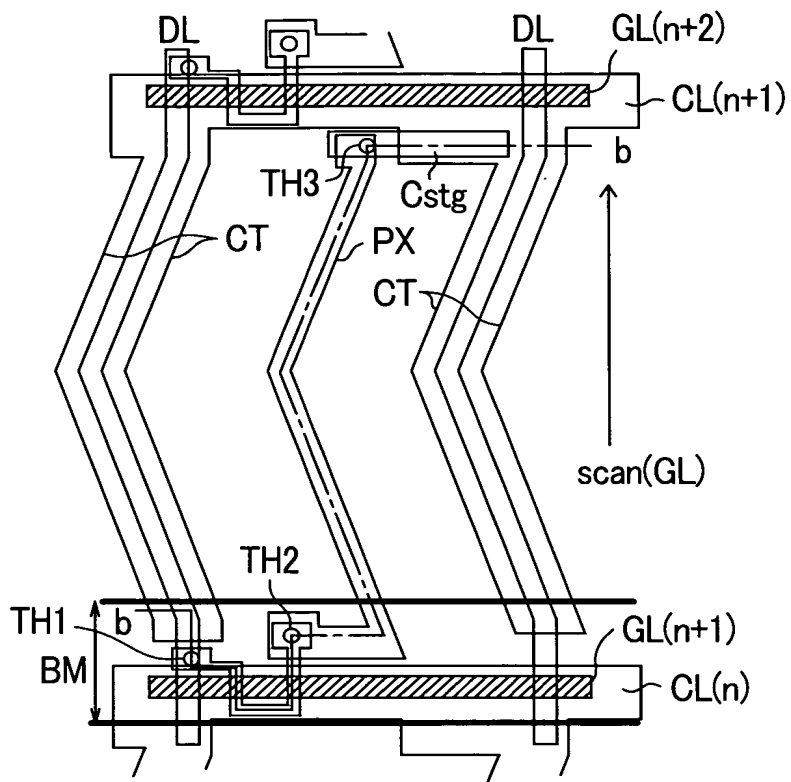
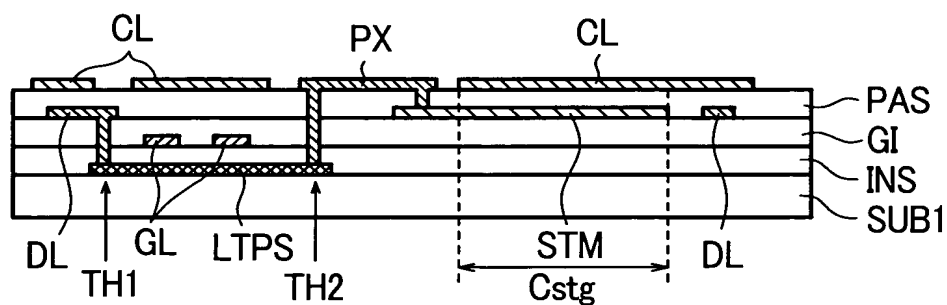


FIG. 21C

GL(n)	ON	OFF	FT	FT
GL(n+1)	FT	ON	OFF	FT
GL(n+2)	FT	FT	ON	OFF
GL(n)	ON	FT	FT	FT
CL(n+1)	FT	ON	FT	FT
CL(n+2)	FT	FT	ON	FT

FIG. 21B



[illegible]

CL PX TH3 CL PAS
DL TH1 GL LTPS TH2 CLA DL GI INS
SUB1
Cstg

FIG. 23A

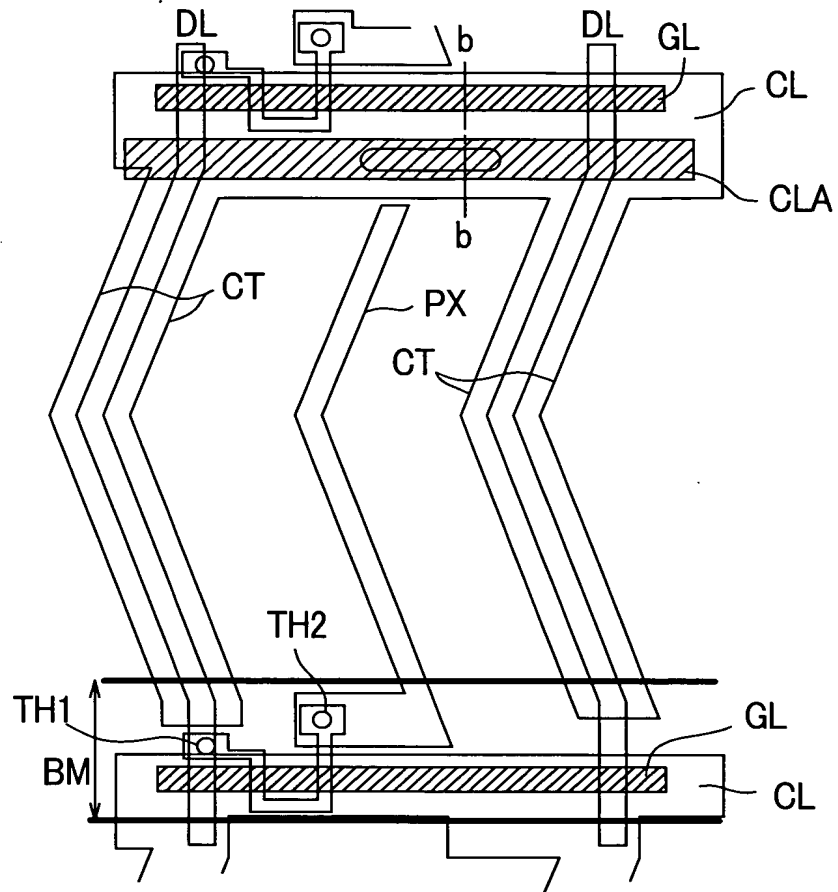


FIG. 23B

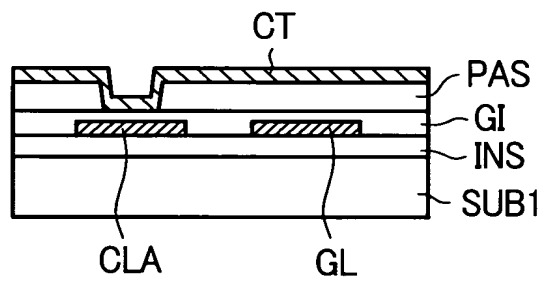


FIG. 23C

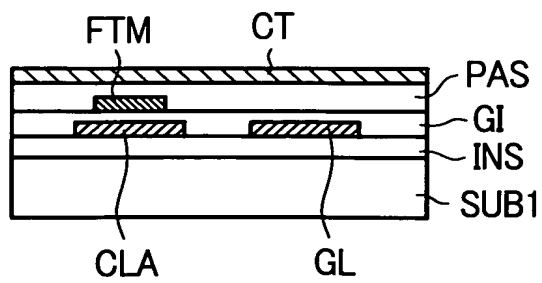


FIG. 24

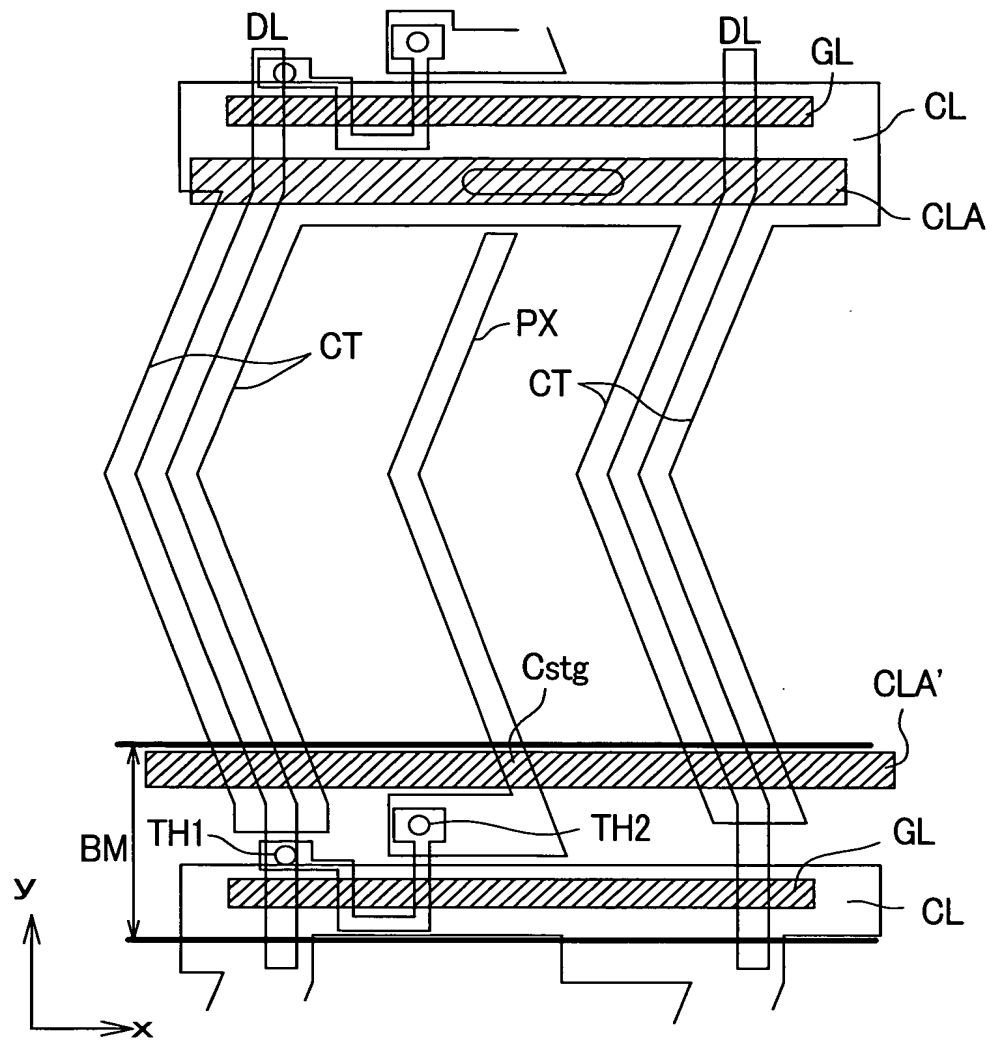


FIG. 25A

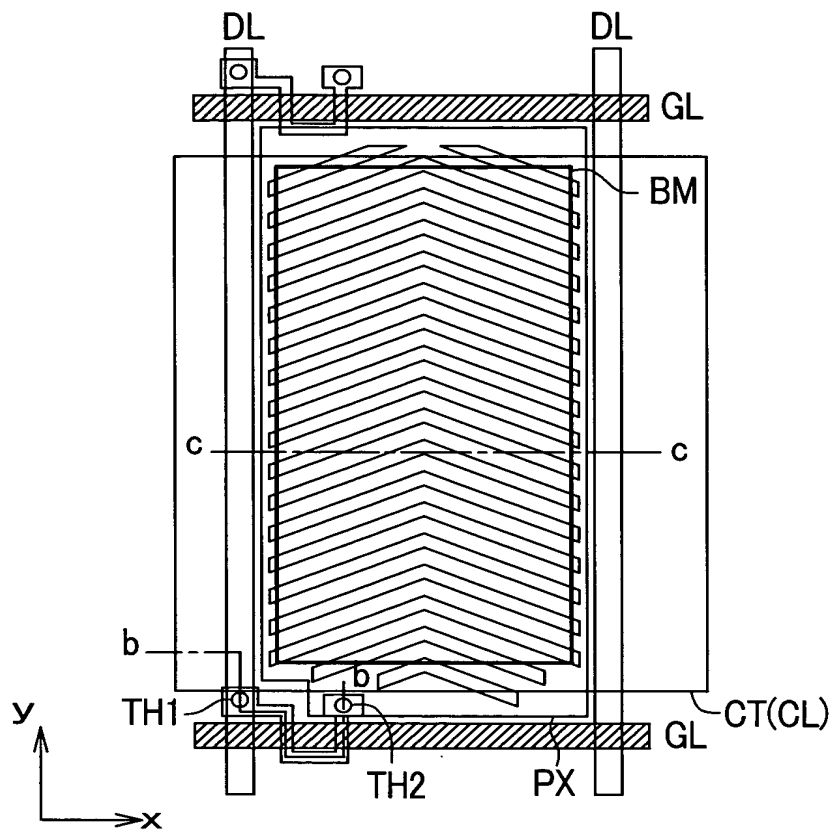


FIG. 25B

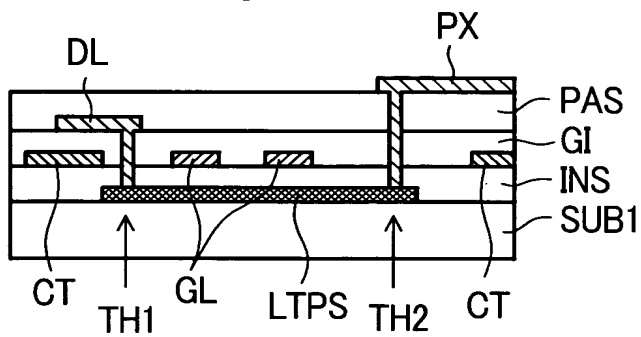


FIG. 25D

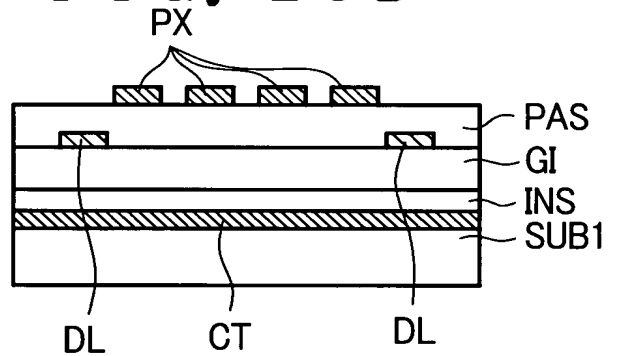


FIG. 25C

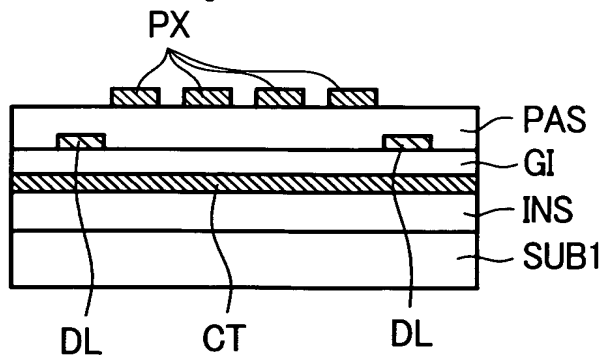


FIG. 26A

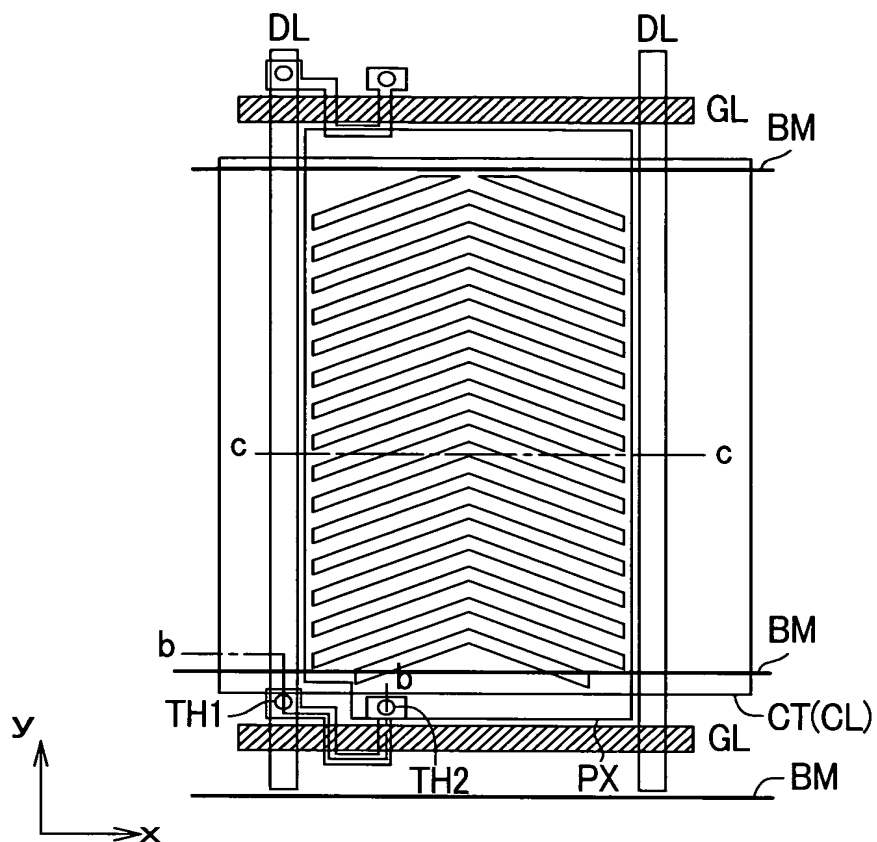


FIG. 26B

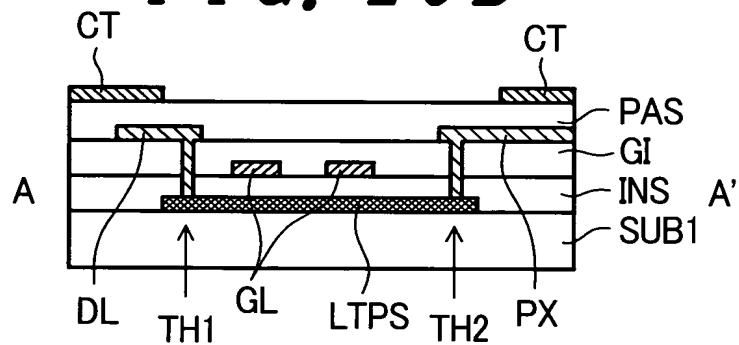


FIG. 26C

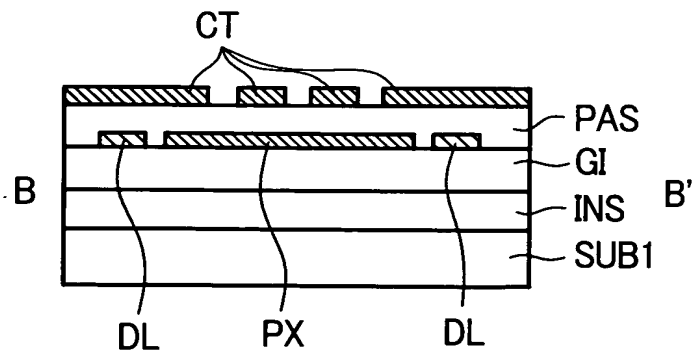


FIG. 27A

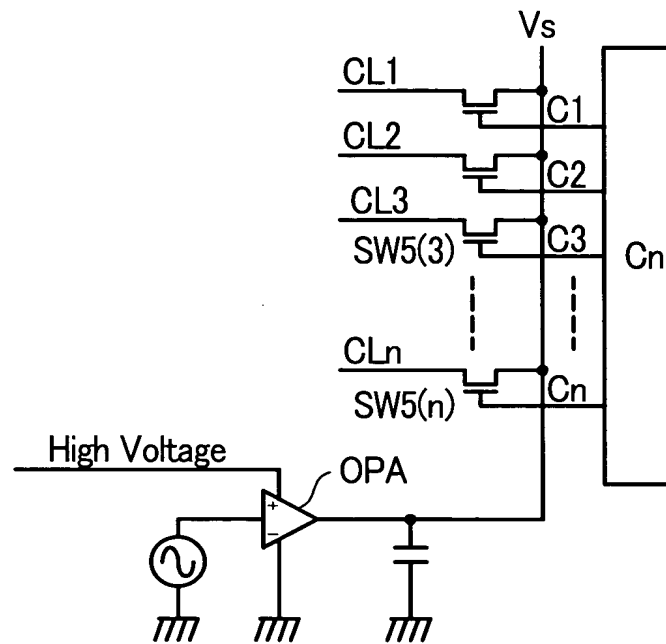


FIG. 27B

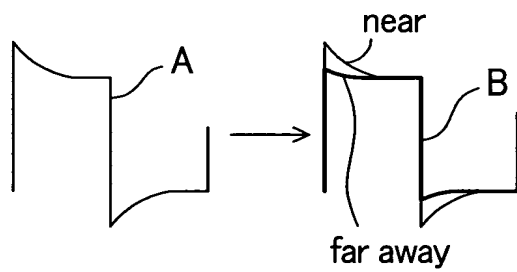


FIG. 27C

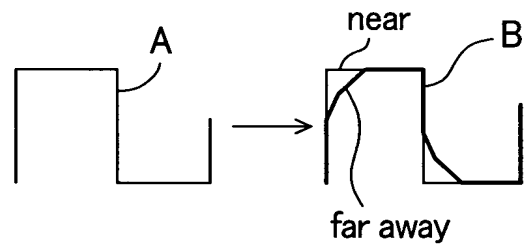


FIG. 28A

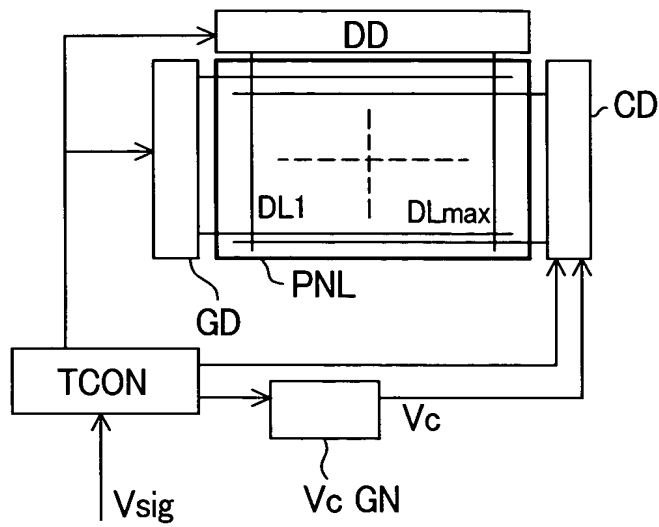


FIG. 28C

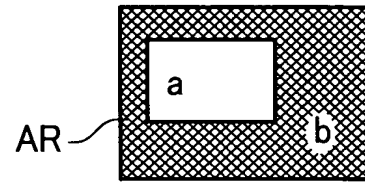


FIG. 28B

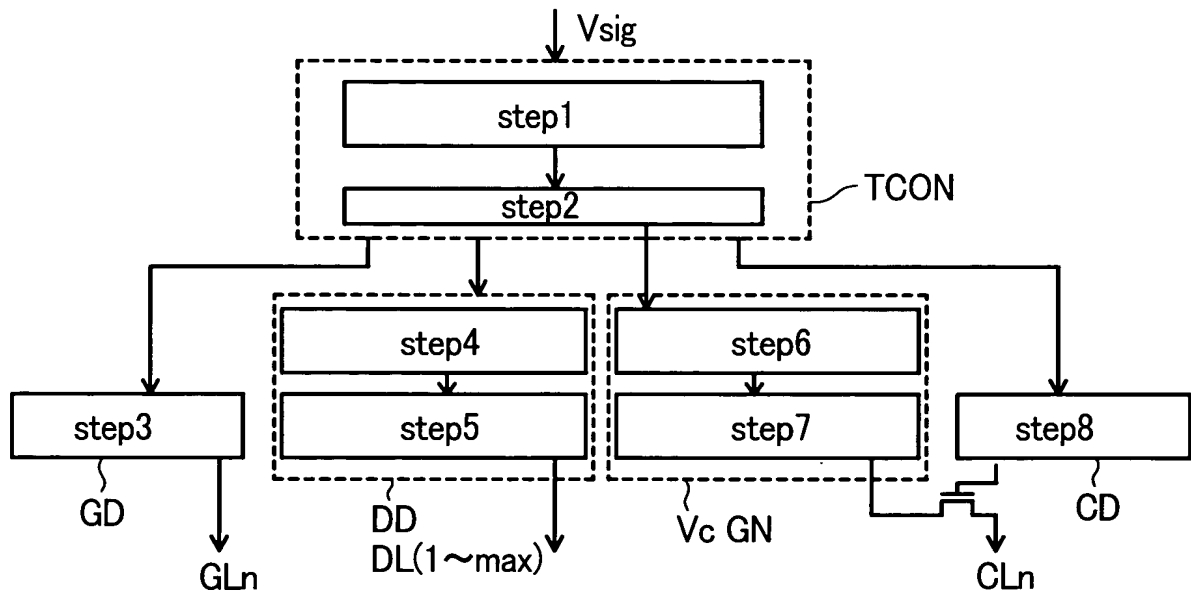


FIG. 29A

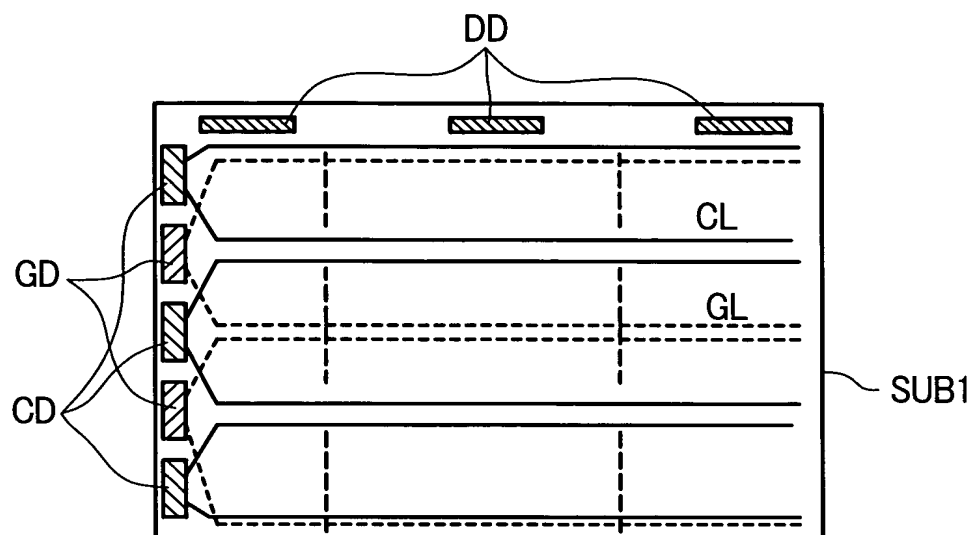


FIG. 29B

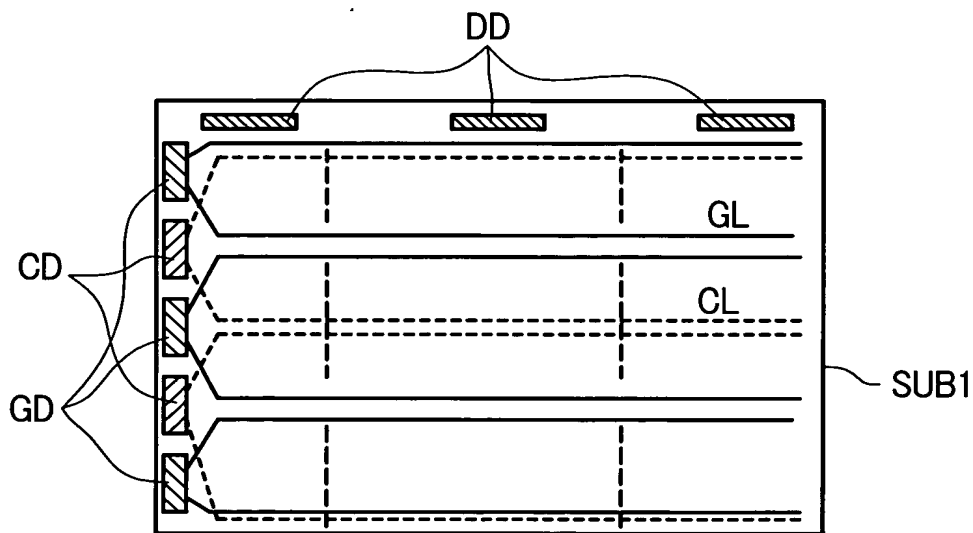


FIG. 30A

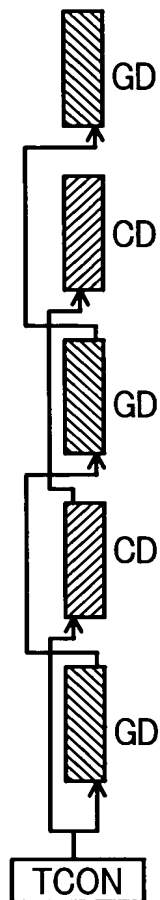


FIG. 30B

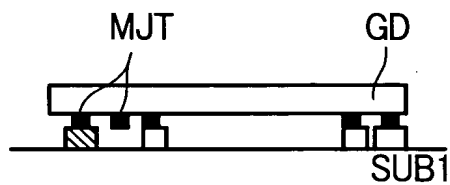


FIG. 30C

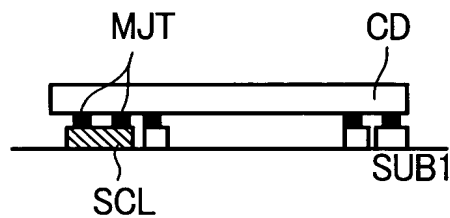


FIG. 30D

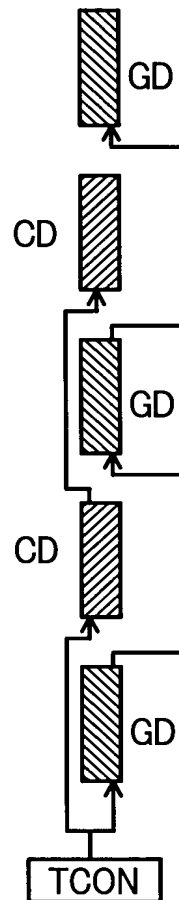


FIG. 31A

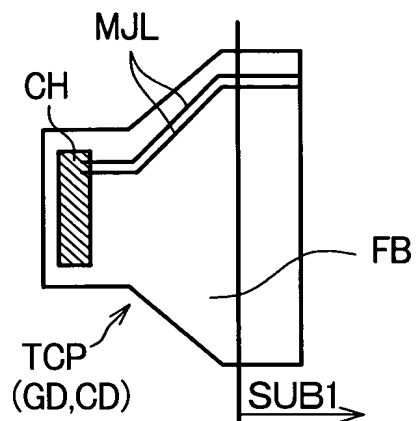


FIG. 31B

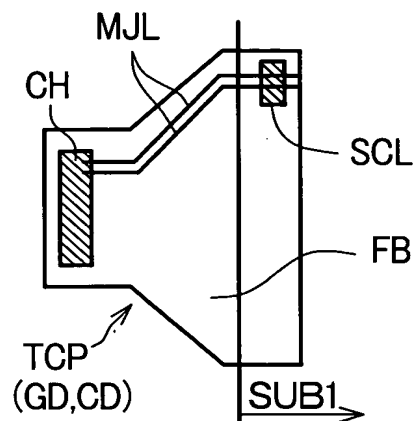


FIG. 31C

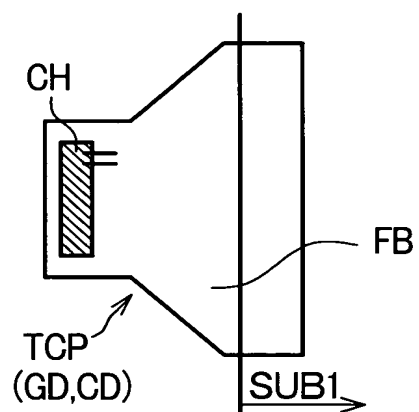


FIG. 31D

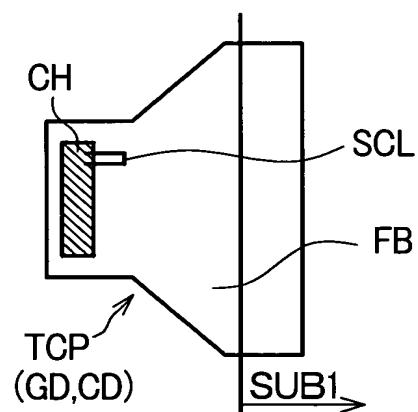


FIG. 32A

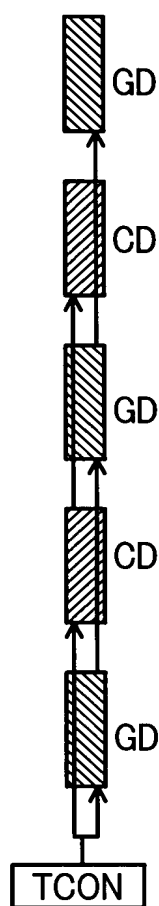


FIG. 32B

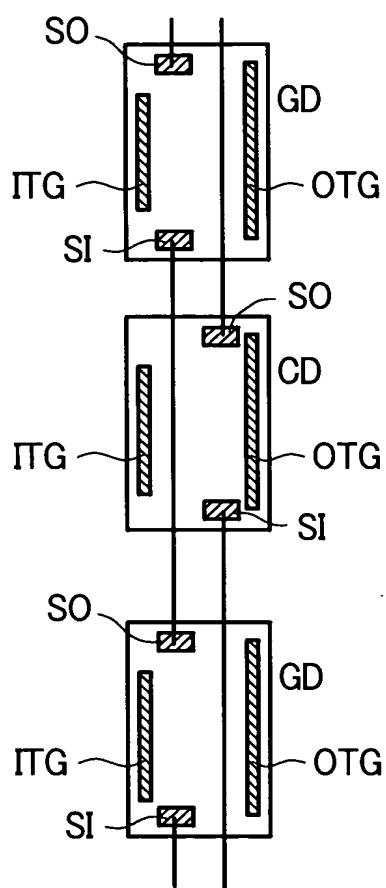


FIG. 32C

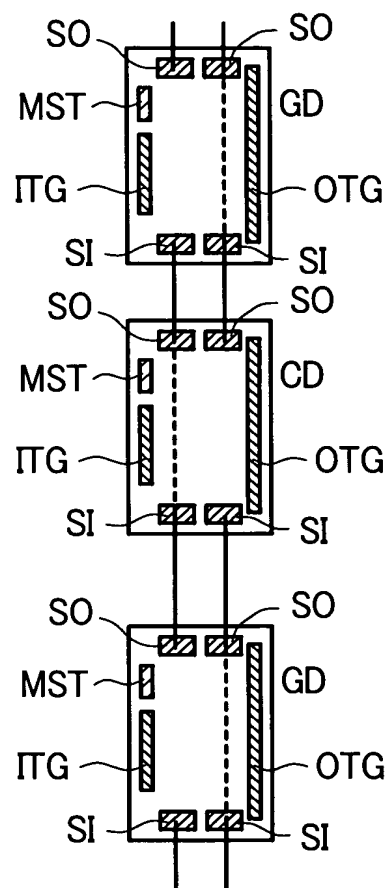


FIG. 32F

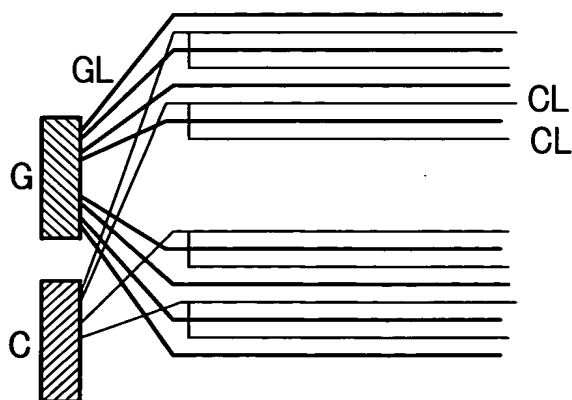


FIG. 32D

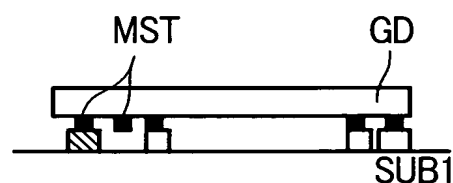


FIG. 32E

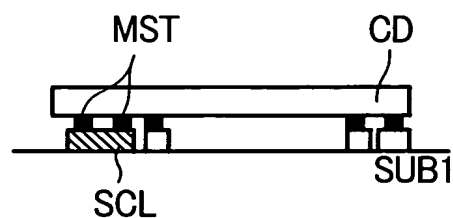


FIG. 33A

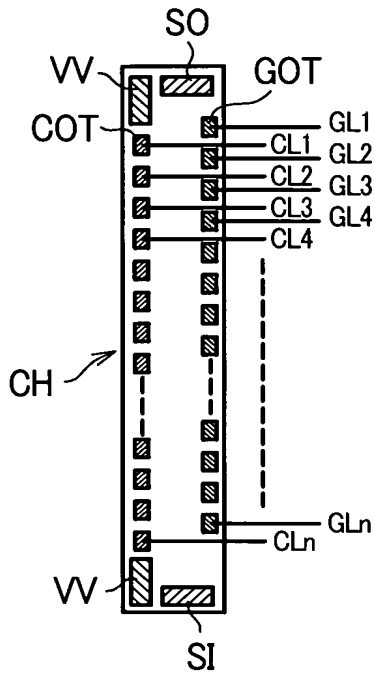


FIG. 33B

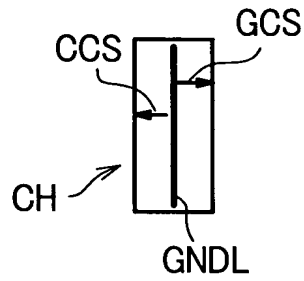


FIG. 33C

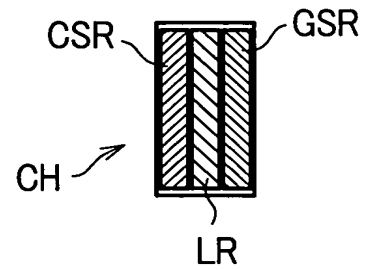


FIG. 33D

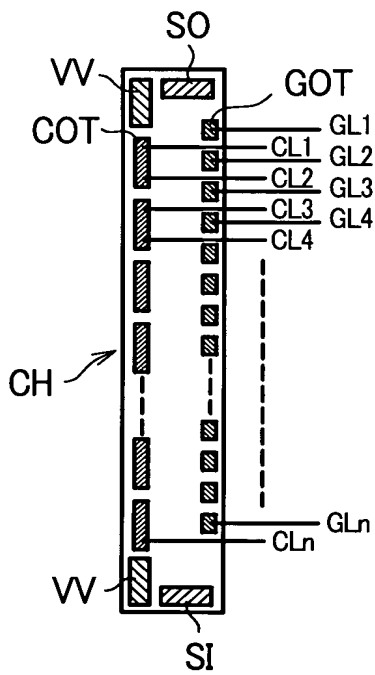


FIG. 33E

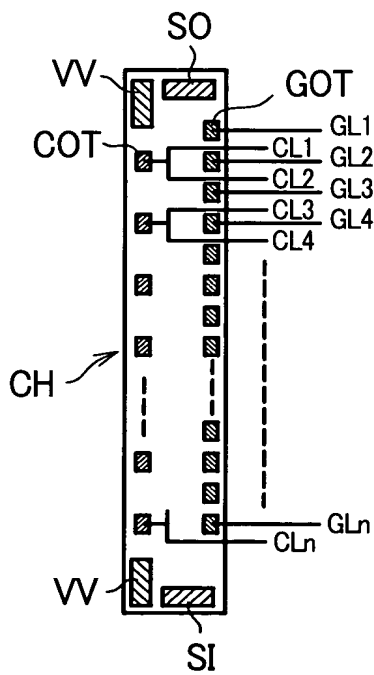


FIG. 33F

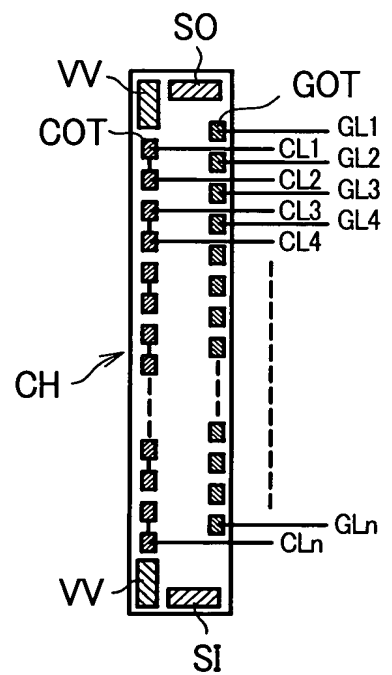


FIG. 34A

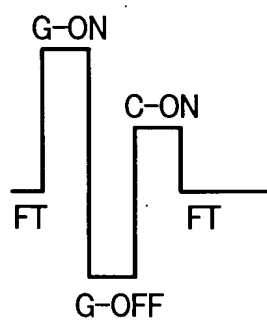


FIG. 34B

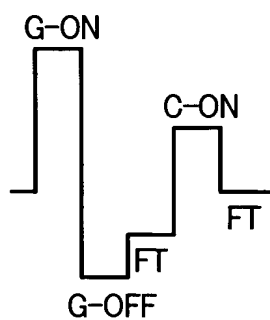


FIG. 34C

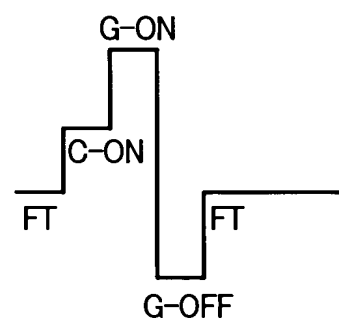


FIG. 35A

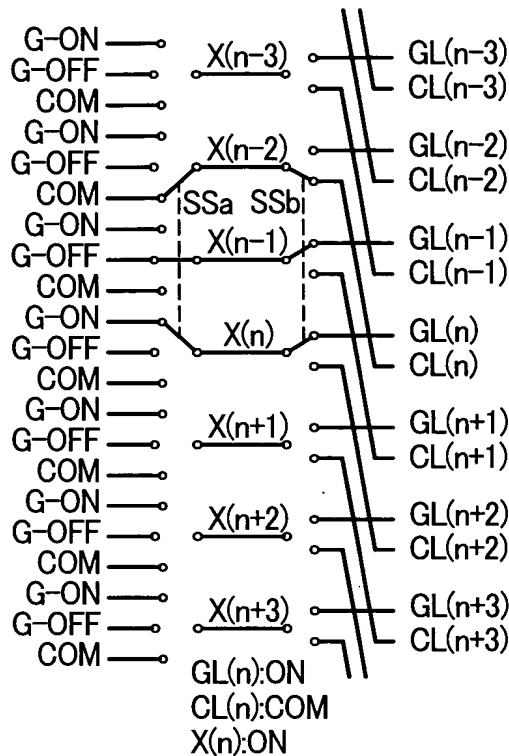


FIG. 35B

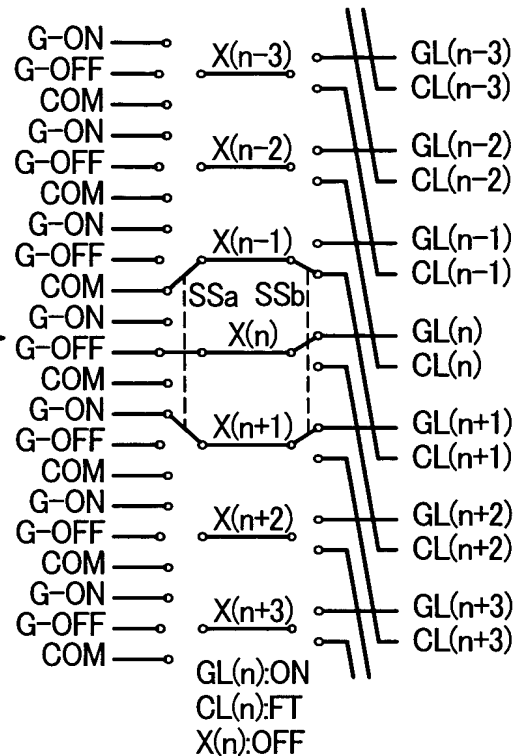


FIG. 35C

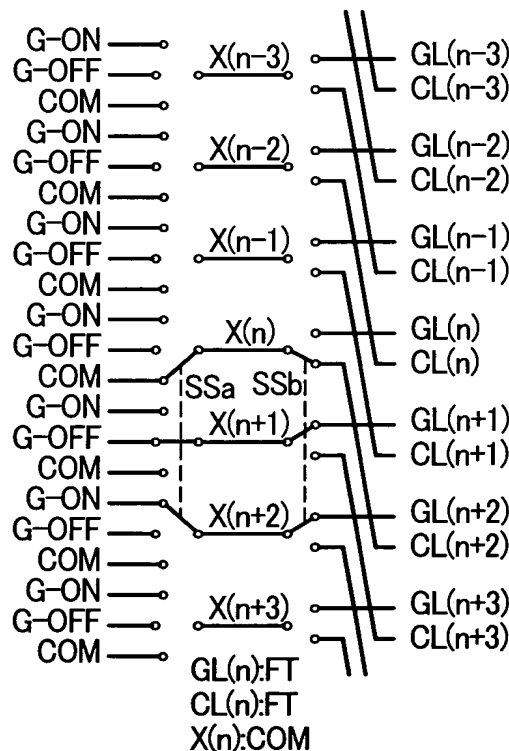


FIG. 35D

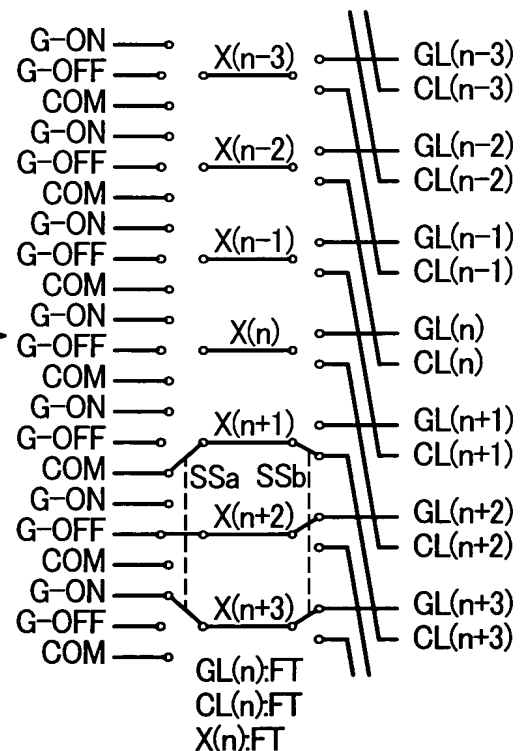


FIG. 36A

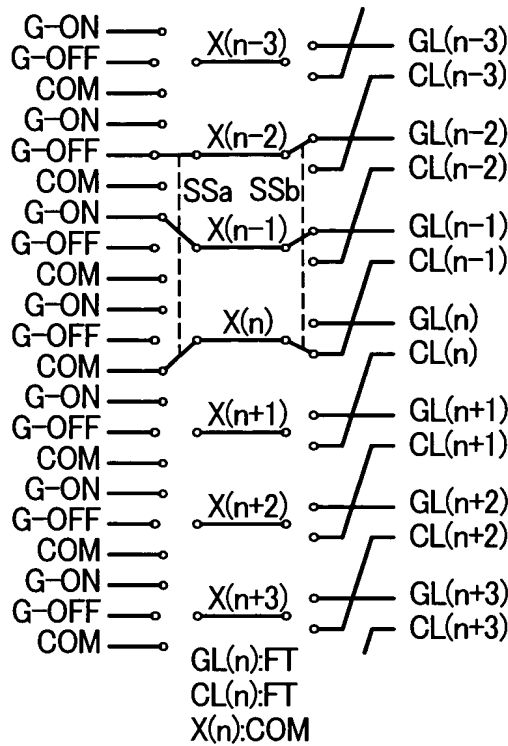


FIG. 36B

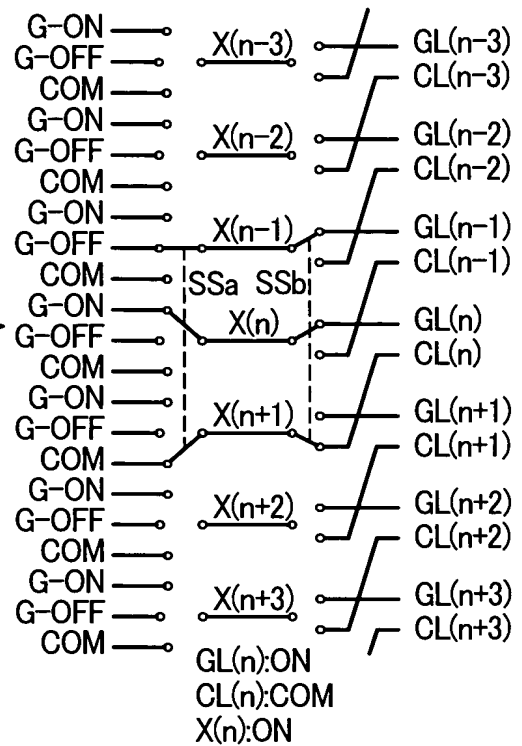


FIG. 36C

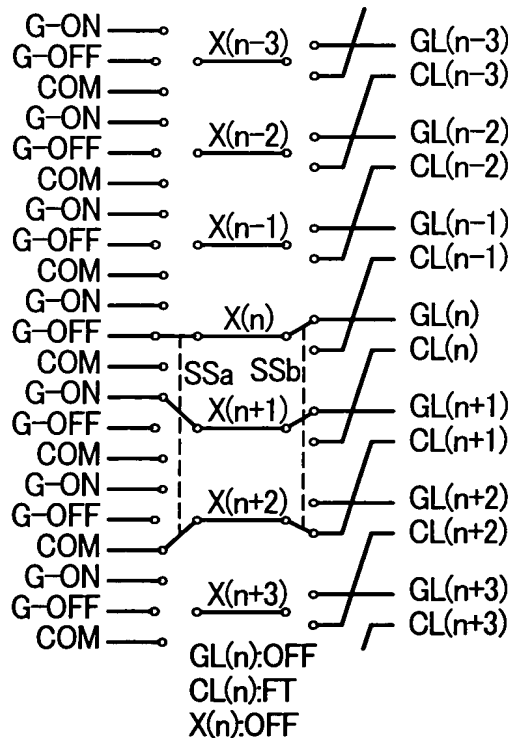


FIG. 36D

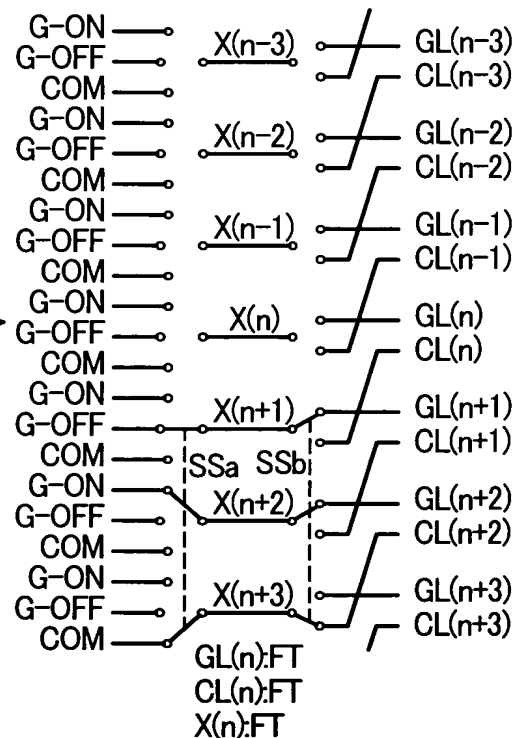


FIG. 37A

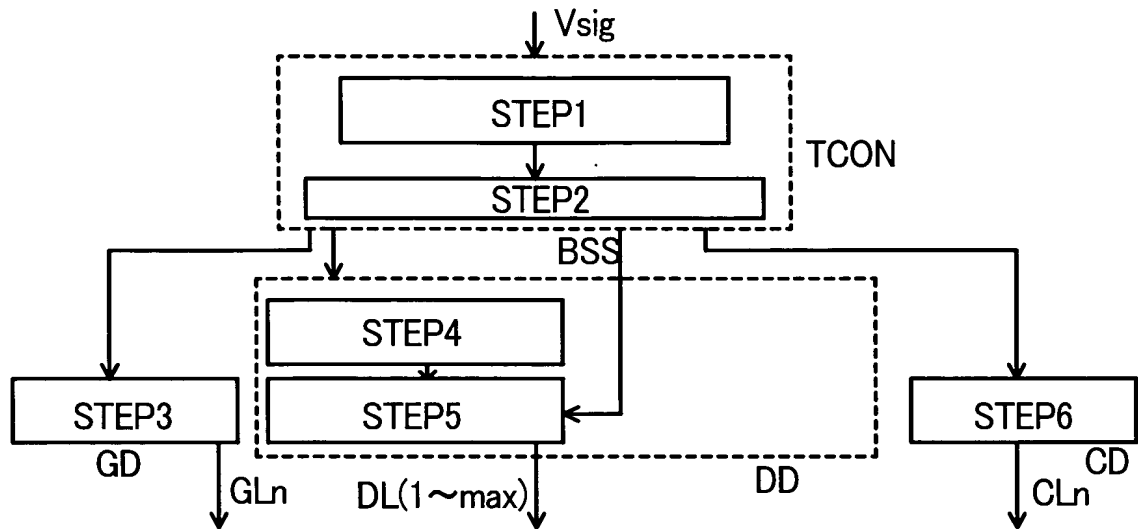


FIG. 37B

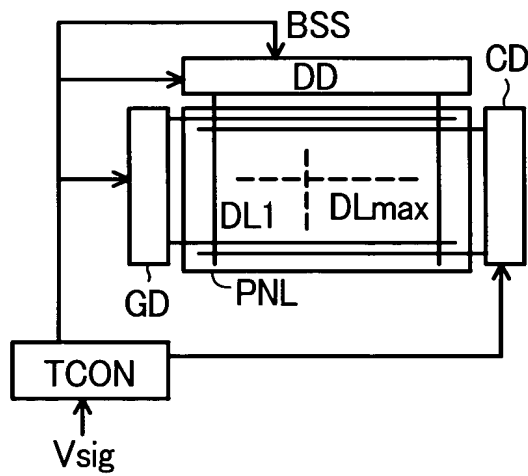


FIG. 37C

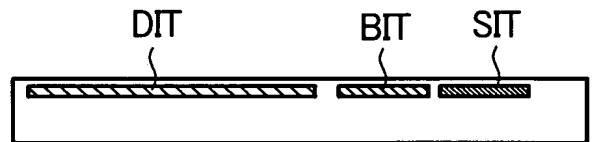


FIG. 37D

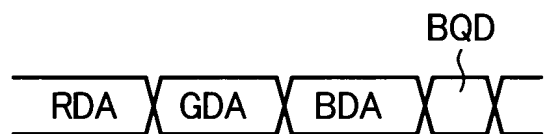


FIG. 38A

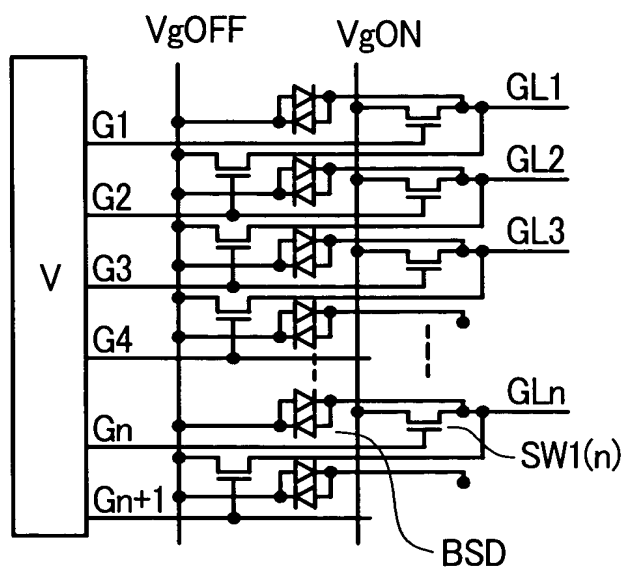


FIG. 38B

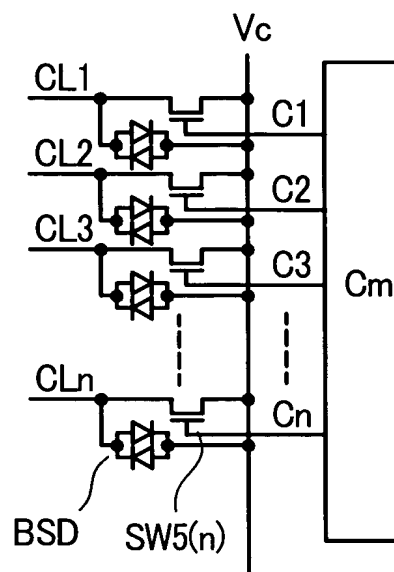


FIG. 39A

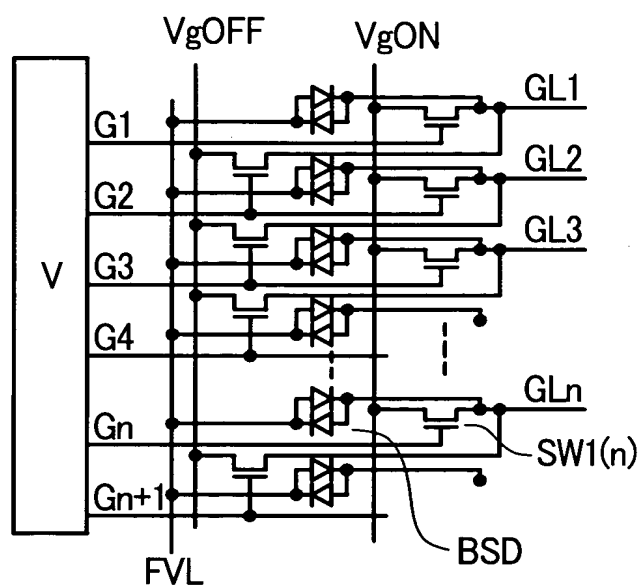


FIG. 39B

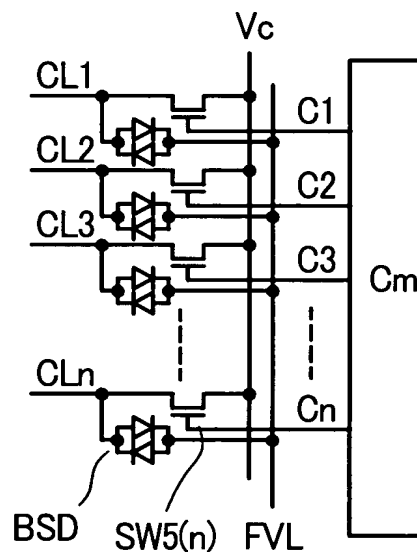


FIG. 40

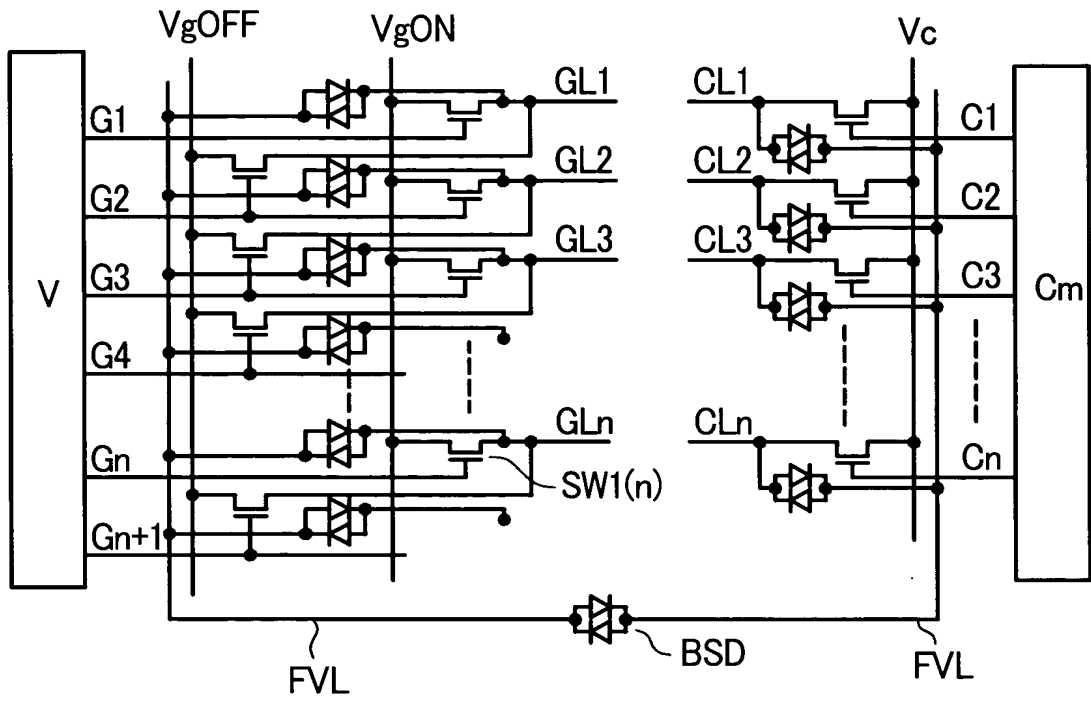


FIG. 41

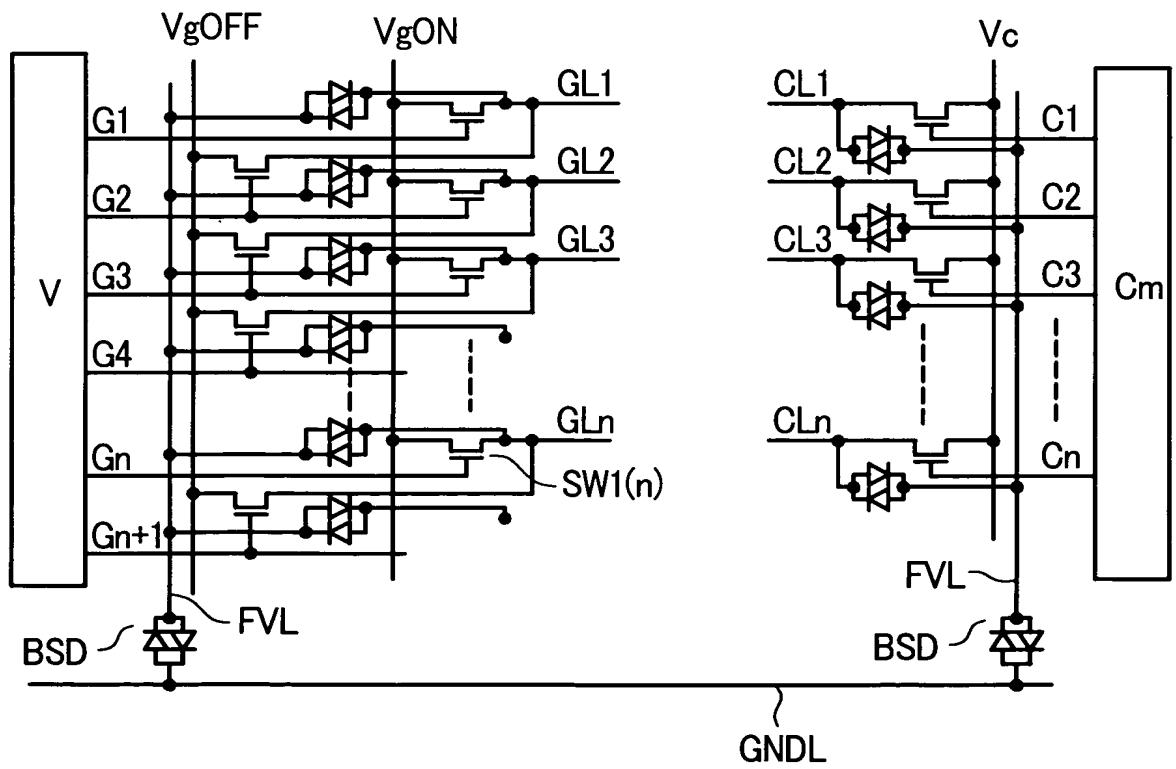


FIG. 42A

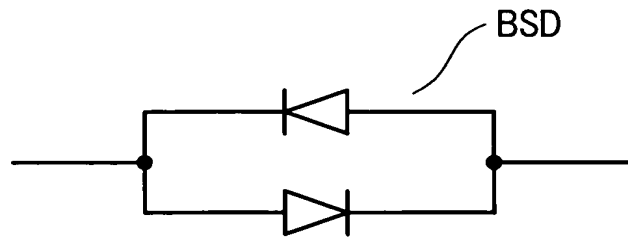


FIG. 42B

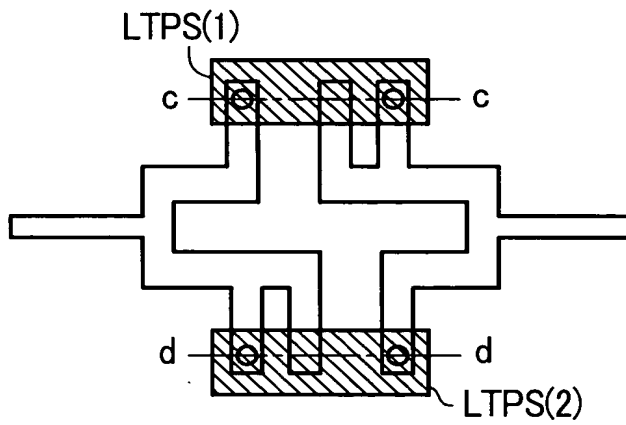


FIG. 42C

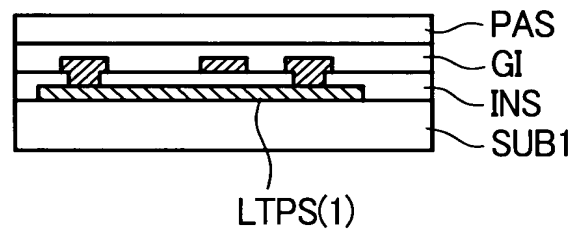


FIG. 42D

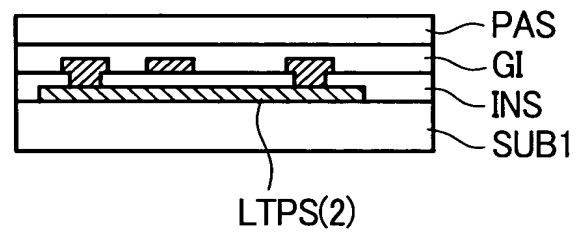


FIG. 43A

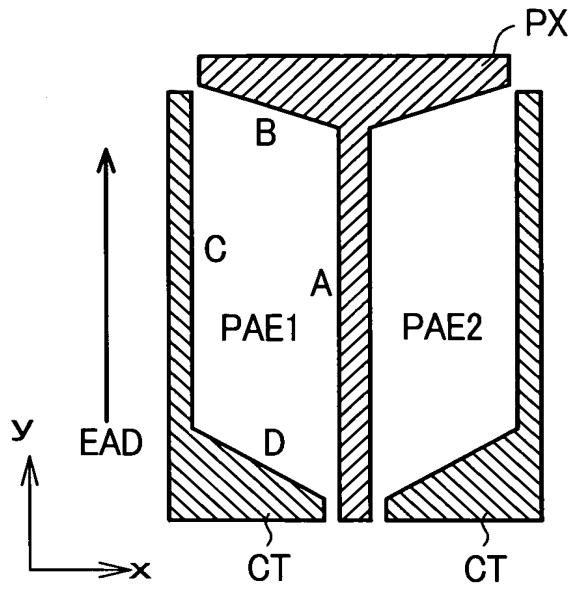


FIG. 43B

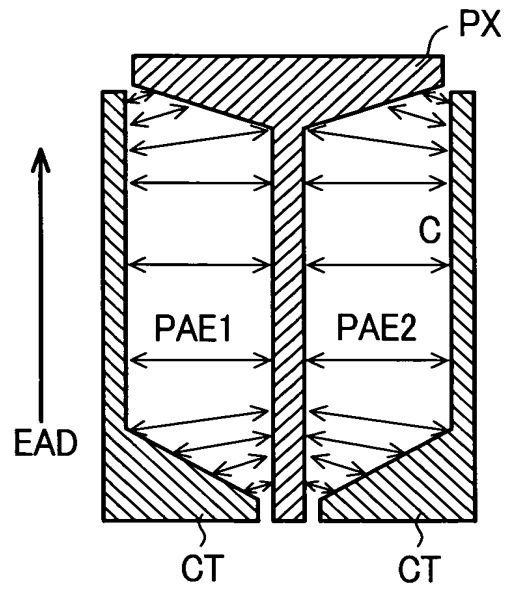


FIG. 43D

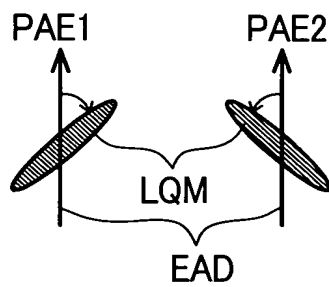


FIG. 43C

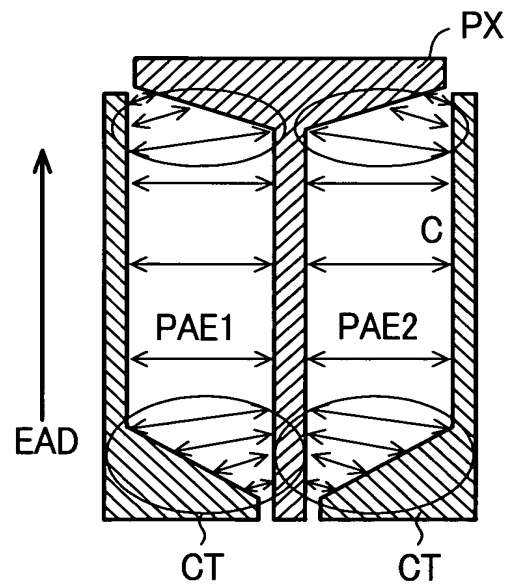


Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate SUB1 with an insulating layer INS on top. A gate layer GL is formed on the insulating layer. A gate oxide layer PAS is formed on the gate layer. A gate electrode CT is formed on the gate oxide layer. A gate insulating layer GI is formed on the gate electrode. A gate contact layer DL is formed on the gate insulating layer. A gate contact layer TH1 is formed on the gate contact layer. A gate contact layer TH2 is formed on the gate contact layer. A gate contact layer PX is formed on the gate contact layer. A gate contact layer PSI is formed on the gate contact layer.

FIG. 45A

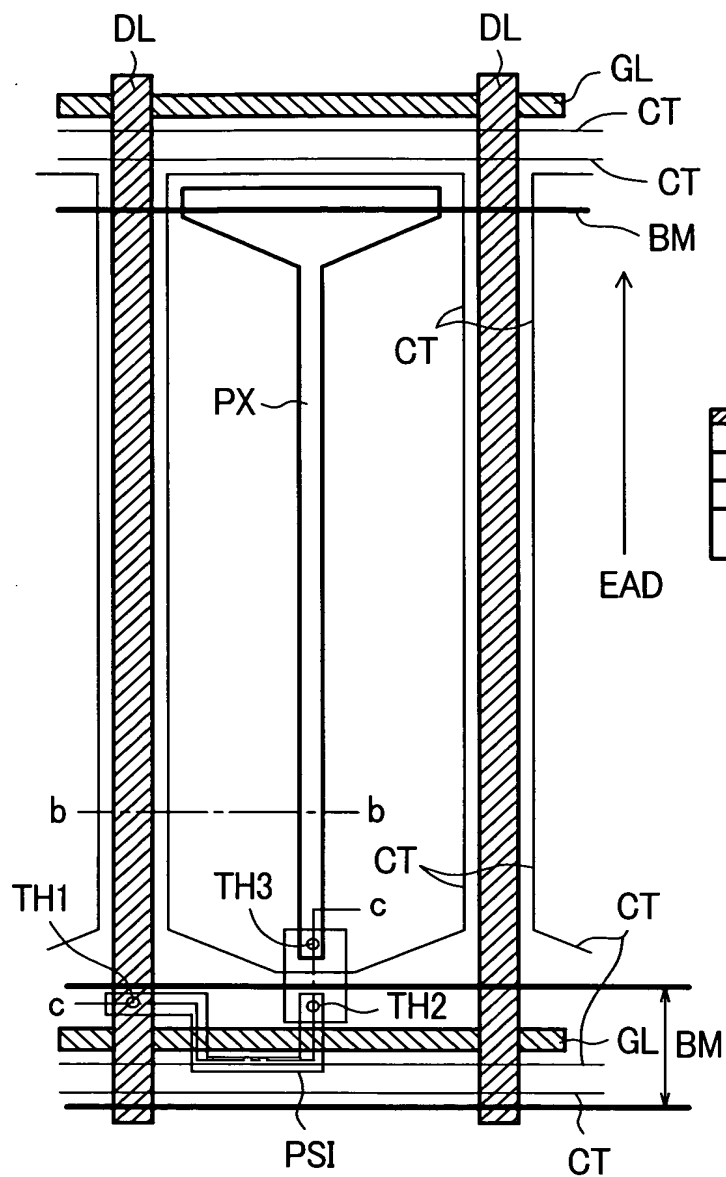


FIG. 45B

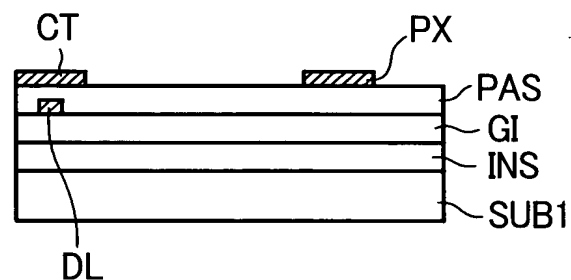


FIG. 45C

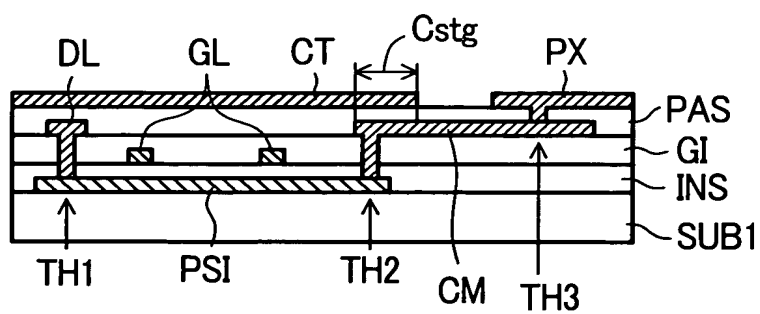


FIG. 46A

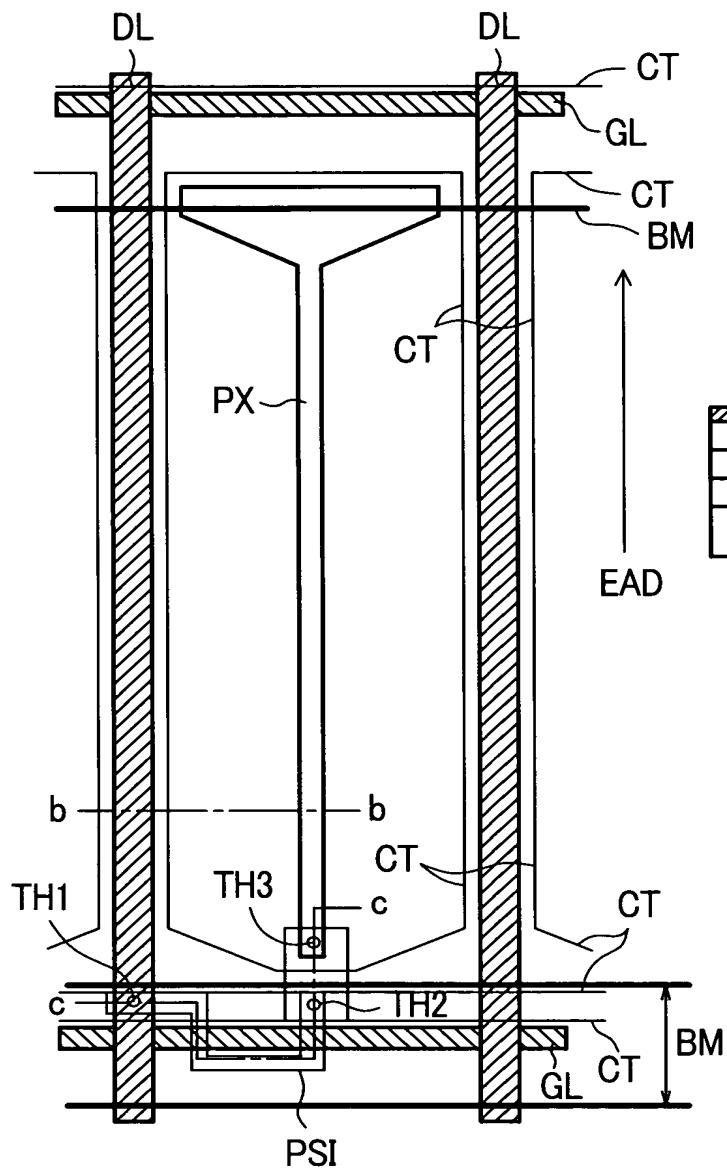


FIG. 46B

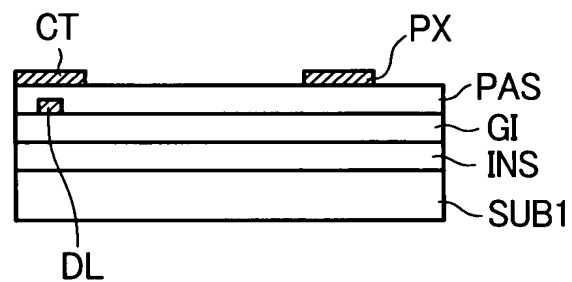


FIG. 46C

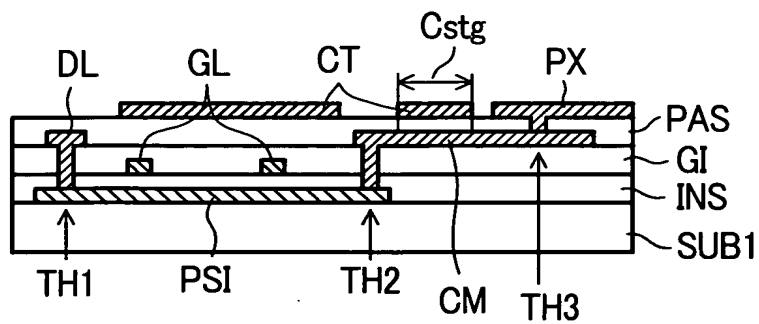


FIG. 47A

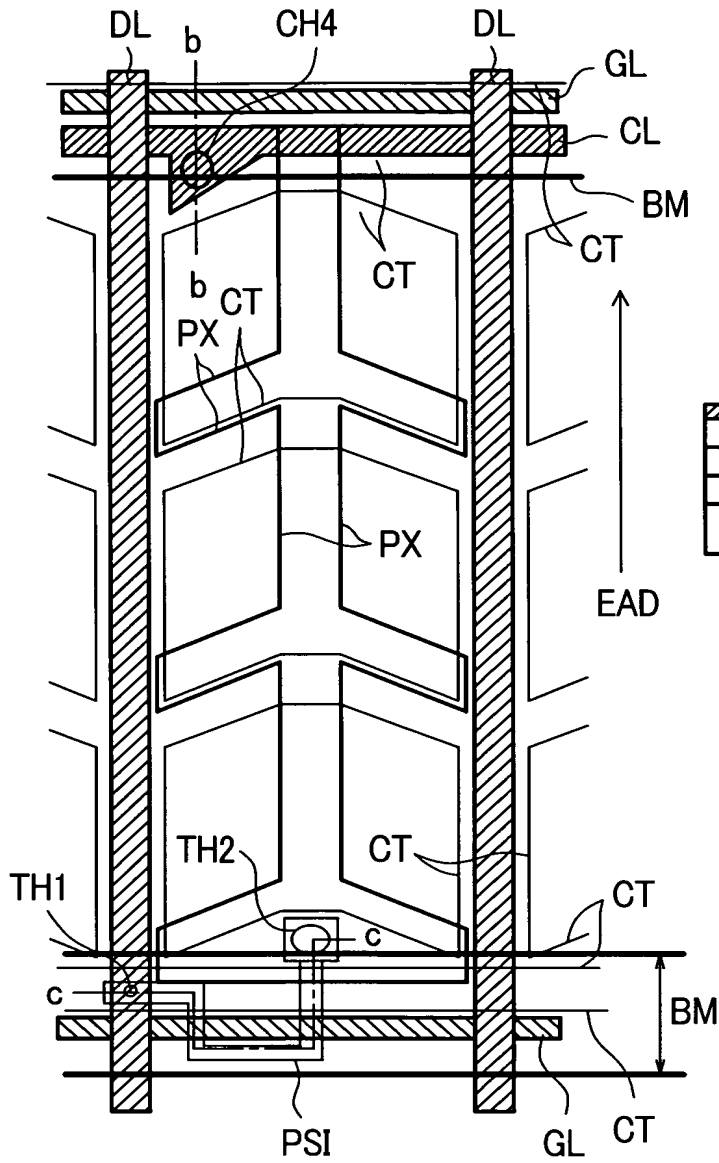


FIG. 47B

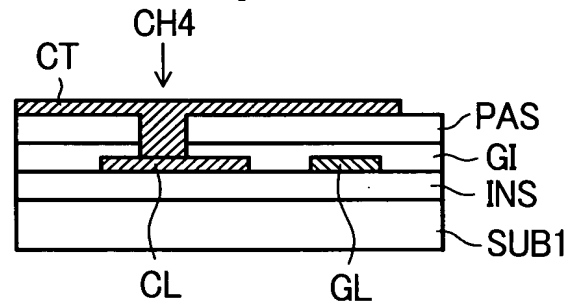
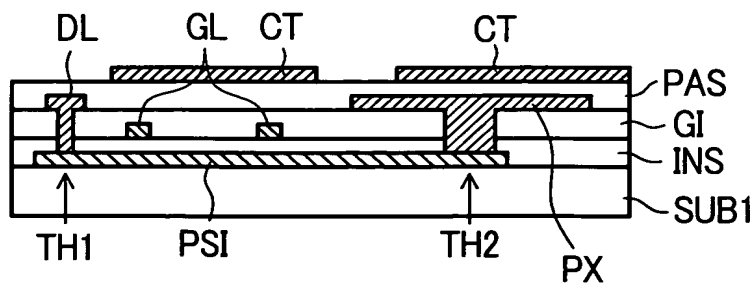


FIG. 47C



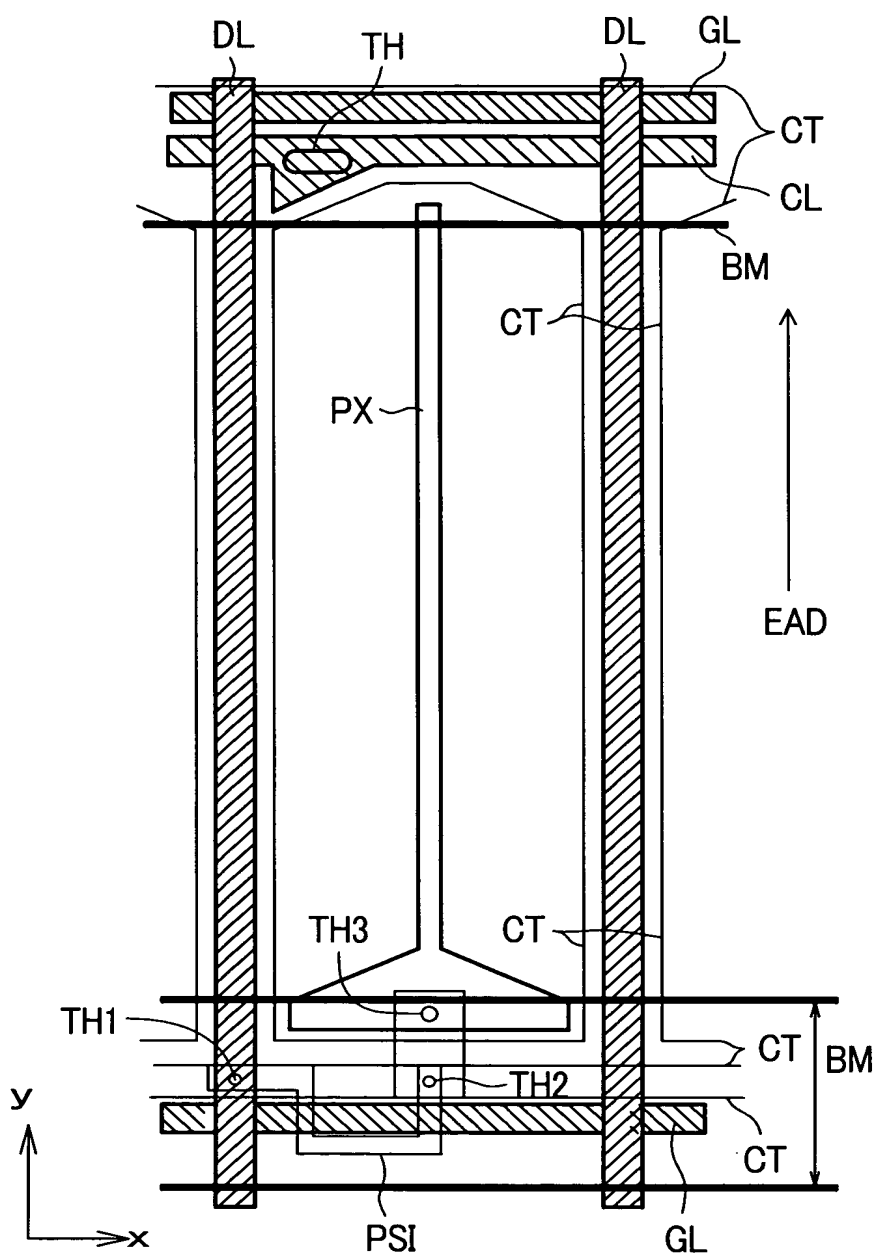


FIG. 49

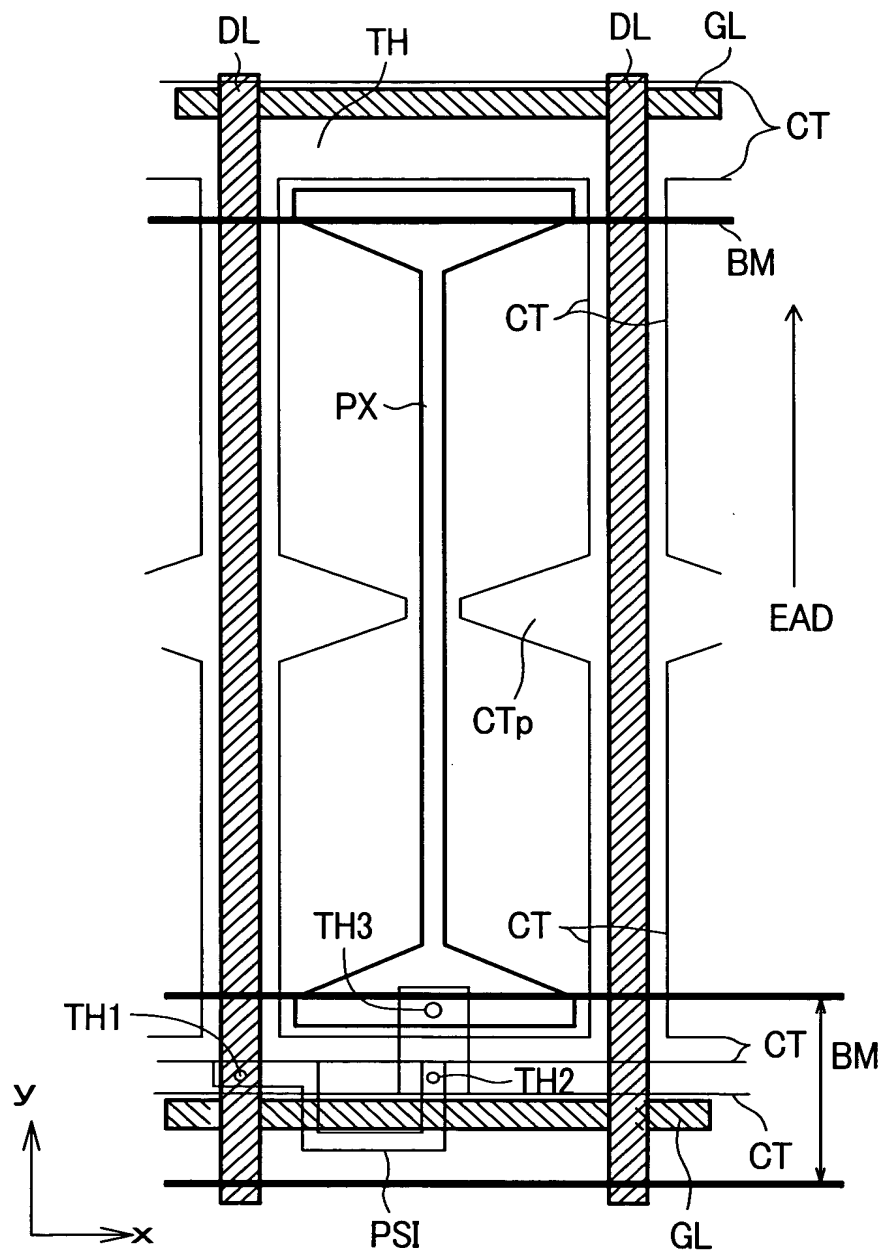


FIG. 50

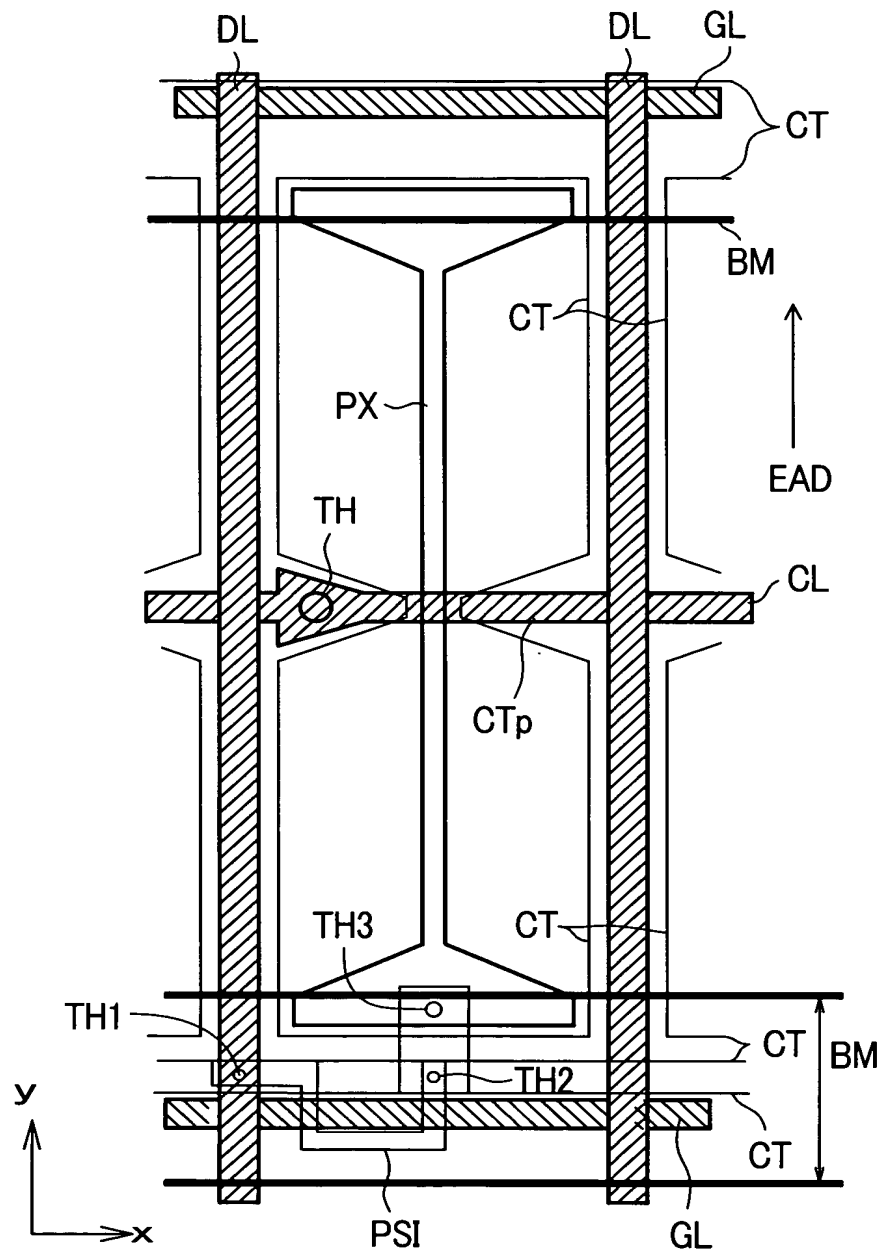


FIG. 51

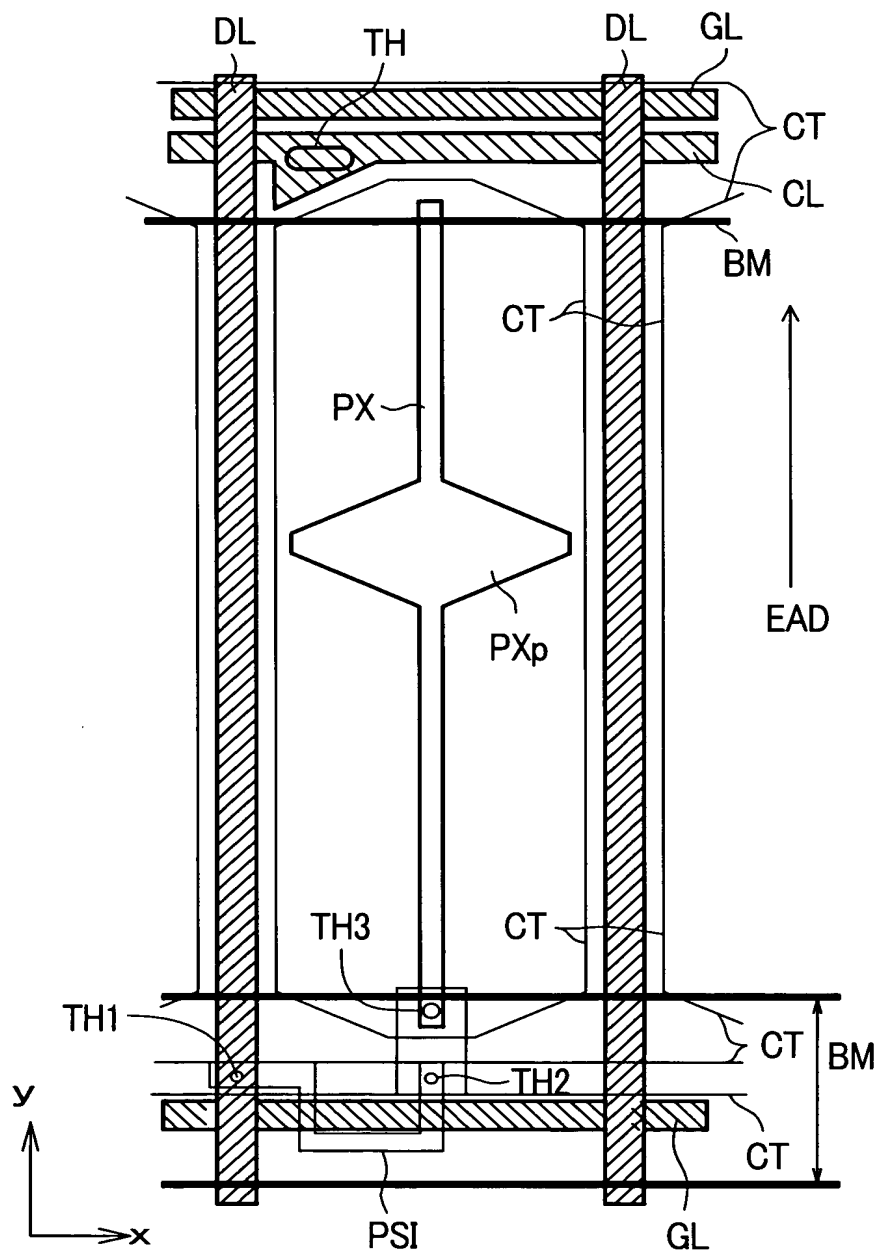


FIG. 52

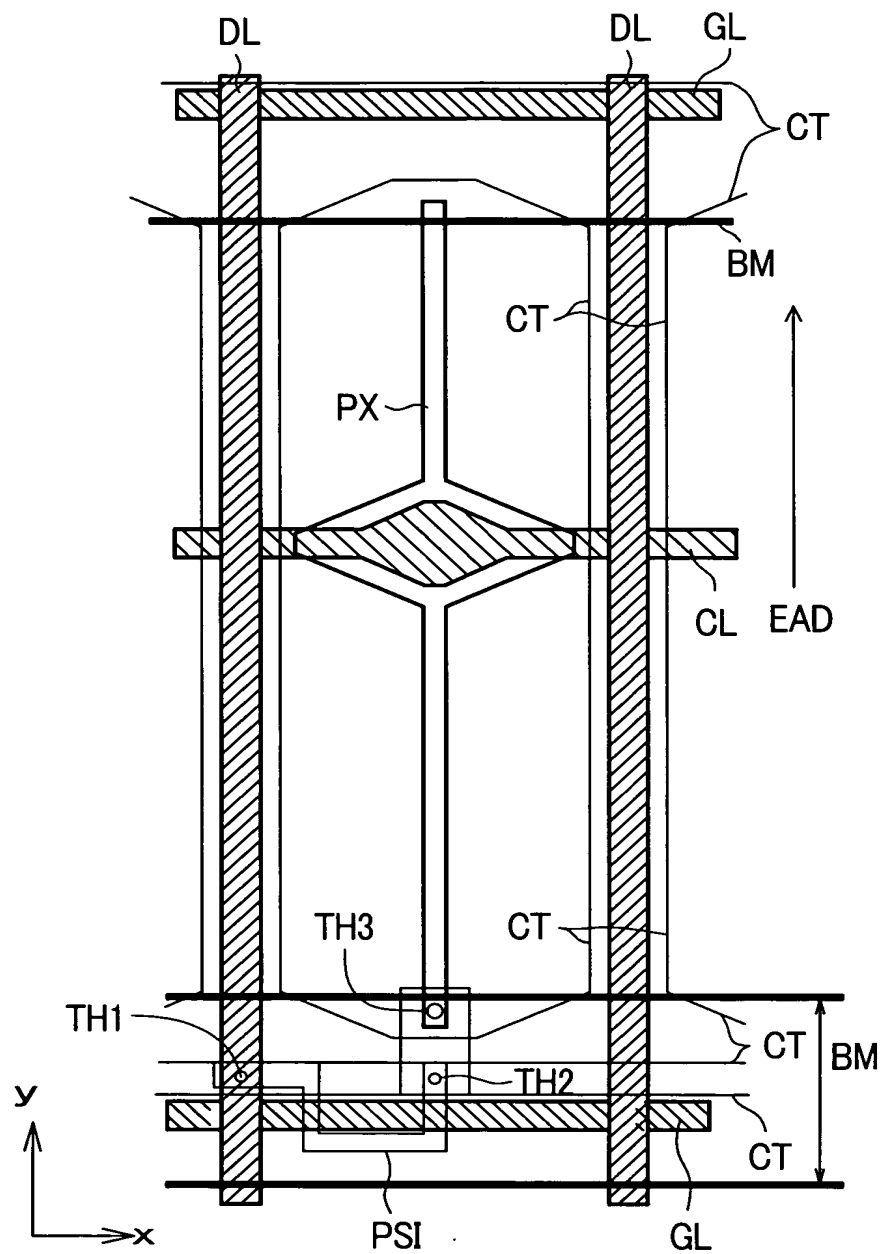


FIG. 53

